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LUNAR EXCURSION MODULE

PRIMARY GUIDANCE, NAVIGATION, AND CONTROL SYSTEM MANUAL

VOLUME II

AC ELECTRONICS
DIVISION OF GENERAL MOTORS
MILWAUKEE, WISCONSIN

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PRIMARY GUIDANCE, NAVIGATION, AND CONTROL SYSTEM MANUAL

VOLUME II OF II

PREPARED FOR

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
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BY

AC ELECTRONICS
DIVISION OF GENERAL MOTORS
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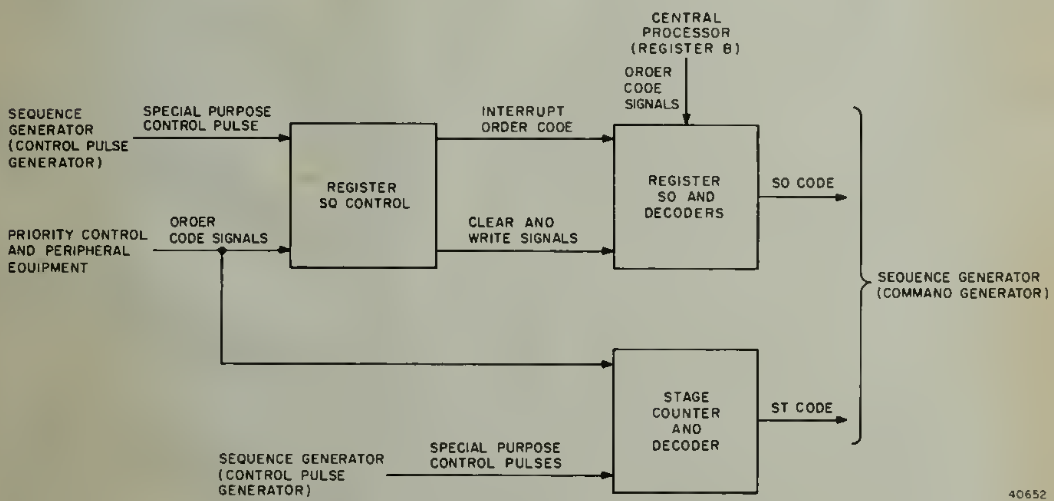


Figure 4-125. Order Code Processor, Block Diagram

Register SQ is a seven-bit register with only six of its bit positions (16 and 14 through 10) connected to the central processor write lines. The seventh (high-order) bit position is the extend bit. This high-order bit position is used for extending the order code field; it contains a logic ZERO for basic instructions and a logic ONE for extracode, channel, and interrupt instructions. Bit positions 16, 14, and 13 produce the SQ signals. At any time, only one of the eight possible SQ signals is present to indicate the octal number specified by these bit positions. Bit positions 12 and 11 contain the quarter code. These bits are decoded into one of four QC signals to indicate the octal number specified by these two bit positions. Bit position 10 is not used for basic and extracode instructions; however, it is used for the channel and interrupt instructions.

The stage counter is a three-stage Gray counter especially adapted for various counts other than the Gray code. Most instructions are several MCT's long and use the two low-order bits of the stage counter. The stage counter controls the length of each instruction. The stage counter always starts an instruction with count 000. Then it may be advanced to 001, 010, or 011 by special purpose control pulses ST1 and ST2 from the control pulse generator. The Gray code count is used for the divide instruction. Control pulse DVST advances the counter through the states 000, 001, 011, 111, 110, and 100. Then control pulse ST2 sets the stage counter to 010 to complete the divide instruction. The content of the stage counter is decoded into the ST code signals. Some of the ST code signals reflect the standard binary count from octal 0 through 3, and others reflect the Gray code count of octal 0, 1, 3, 7, 6, and 4. The order code signals from the priority control and the peripheral equipment set the stage counter to a particular state in a manner similar to that in which register SQ is set. The interrupt order code signal sets the stage counter to 000, the start order code signal sets it to 001, and the transfer control to specified address signal sets it to 011. The outputs of register SQ and stage decoders are sent to the command generator where they are used to produce subinstruction and instruction commands.

4-5.4.2 Command Generator. The command generator (figure 4-126) contains the subinstruction decoder, instruction decoder, and the counter and peripheral instruction control. The subinstruction decoder receives the SQ and ST code signals from the order code processor. These signals represent the order codes of all machine instructions and are decoded into subinstruction and instruction commands. For example, channel instruction WOR has a binary order code 1 000 101 and stage code 000. The SQ code signals SQEXT, SQ0, QC2, and SQR10 are combined with ST code signal ST0 to produce subinstruction command WOR0.

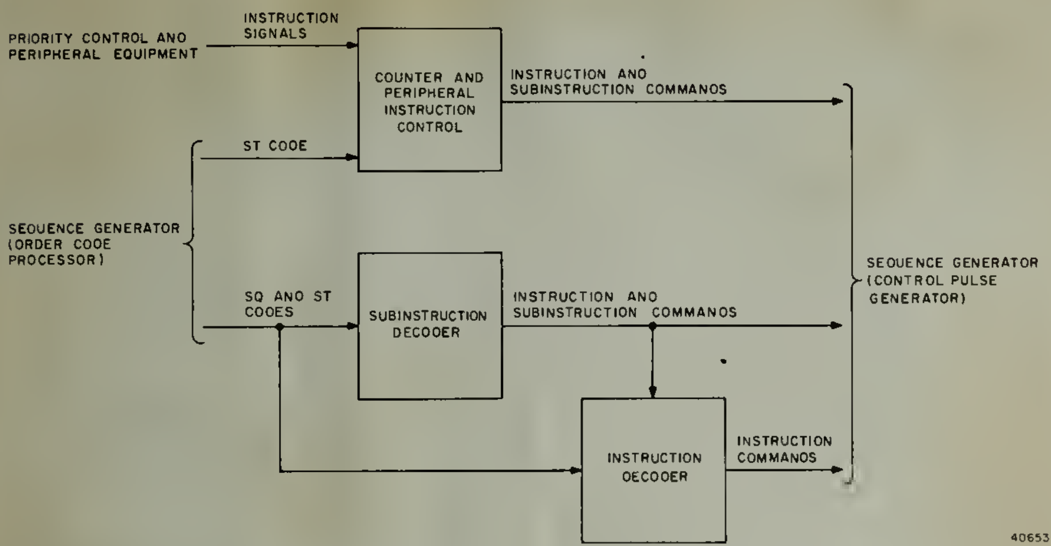


Figure 4-126. Command Generator, Block Diagram

The instruction decoder receives the coded signals from the order code processor in addition to certain subinstruction commands. It produces signals called instruction commands. An instruction command is used for two or more subinstructions as compared to a subinstruction command which is used for only one subinstruction. For example, instruction command IC1 generates a combination of control pulses shared by subinstructions NDX0 and NDXX0. Instruction command IC1 is produced by signals SQEXT, SQ5, and ST0 for subinstruction NDX0 or by signals SQ5, QC0, and ST0 for subinstruction NDXX0. Other instruction commands are produced from subinstruction commands. For example, IC8 is produced by ORing DXCH0 with LXCH0.

The counter and peripheral instruction control receives instruction signals from the priority control and the peripheral equipment. These signals are applied to separate circuits which control the individual counter and peripheral instructions. The instruction signals from the priority control pertain to counter locations and the instruction(s) associated with each location. For example, signal C31A is interpreted as counter 31 address. The content of this location can only be changed by instruction DINC whose subinstruction command is produced by the counter and peripheral instruction control. Another example is signal C42P, interpreted as counter 42 positive increment or signal

C42M, counter 42 negative increment. The peripheral equipment supplies instruction signals such as MREAD and MLOAD for the fetch and store instructions, respectively. While the particular instruction is being executed, the counter and peripheral instruction control stores the input signals in the same way that order code signals are stored by register SQ. Since some of the peripheral instructions are several MCT's long, they use the ST code signals. The subinstruction and instruction command outputs of the command generator are used by the control pulse generator in conjunction with time pulses T01 through T12 to produce action pulses.

4-5.4.3 Control Pulse Generator. The control pulse generator (figure 4-127) contains the crosspoint generator, control pulse gates, and branch control. The crosspoint generator receives instruction and subinstruction commands from the command generator and branch commands from the branch control. The crosspoint generator produces an action pulse when a command signal and a time pulse are ANDed. This action is called the crosspoint operation. For example, action pulse 5XP12 is produced from subinstruction command DAS0 and time pulse T05. Many instructions use identical action pulses. When this is the case, several command signals such as TC0, TCF0, or IC4 will produce the same action pulse during time period T01. The branch commands are used to change the action pulse that normally is produced at a given time. For example, when certain conditions exist, a branch command will produce action pulse 8XP6 in addition to another action pulse normally produced at time period T08. The action pulses are supplied to the control pulse gates which convert them to specific control pulses for use in instruction execution.

The control pulse gates perform the Boolean NOR function. There is one gate for each control pulse. These gates split the action pulses into as many control pulses as

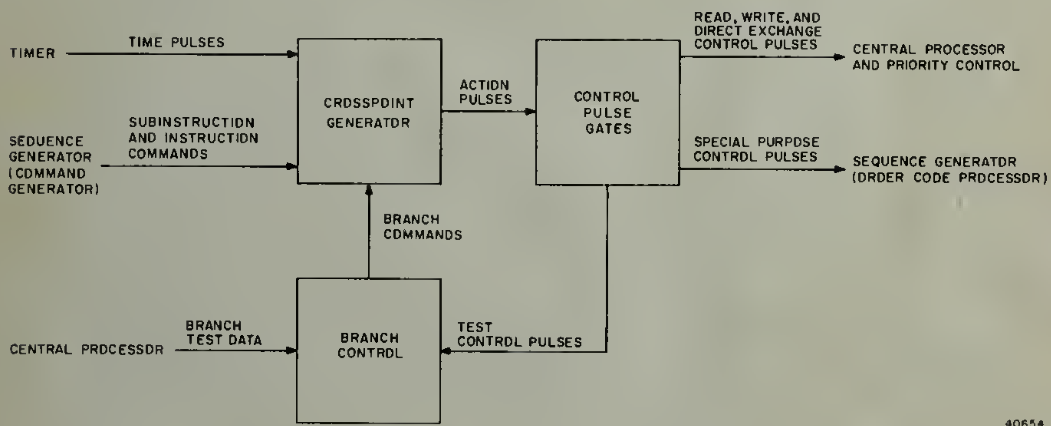


Figure 4-127. Control Pulse Generator, Block Diagram

are required for a particular operation. For example, action pulse 3XP6 is converted to control pulses RZ and WQ. Some of the control pulses produced by the control pulse gates are used by the sequence generator. These include the special purpose control pulses which control the operation of the order code processor and the test control pulses which are applied to the branch control. The other control pulse groups, namely the read, write, and direct exchange control pulses are used in the central processor and the priority control. The purpose of each control pulse is described in paragraph 4-5.2, Machine Instructions.

The branch control is connected to the write lines of the central processor. Data which is placed onto the write lines by read control pulses is tested in the branch control. The branch control contains two stages. Branch 1 normally tests for sign and branch 2 tests for full quantities such as plus or minus zero. Both branches test for positive and negative overflow and have the overflow bits written directly into the branch register. Positive overflow is 01 where branch 1 is the high order bit. Negative overflow is 10. The branch commands sent to the crosspoint generator affect the action pulses at given times. The branch control also contains the special instruction flip-flop which controls the execution of RELINT, INHINT, and EXTEND instructions.

4-5.4.4 Register SQ Control. The register SQ control (figure 4-128) is regulated by special purpose control pulse NISQ from the control pulse generator. Control pulse NISQ causes the register SQ control to produce clear signal CSQG, read signal RBSQ, and write signal WSQG. These signals place the order code (content of register B) onto the write lines and into register SQ at the beginning of each new instruction. The order code signals applied to the register SQ control from the priority control (GOJAM and RUPTOR) and peripheral equipment (MTCSAI) pertain to start, interrupt, and transfer control to specified address instructions, respectively. A distinct priority is associated with each of these three instructions. Interrupt and transfer control to specified address instructions can never be requested when the computer is forcing the execution of the start instruction, which has the highest priority. Certain peripheral instructions occupy the next level of priority, followed by the counter instructions and in turn the transfer control to specified address instruction, which has priority over the interrupt instruction; all six of these instruction categories have priority over basic instructions. In addition, the interrupt instruction cannot be executed when the next instruction being called is an extracode instruction. The register SQ control establishes this priority. It also provides signals to force register SQ to the 0 000 000 state for start and transfer control to specified address instructions, and state 1 000 111 for the interrupt instruction. The register SQ control is able to inhibit the processing of all subsequent interrupts when specified by the program and will permit only one interrupt to be processed at a time. Certain monitor functions built into the register SQ control may be used when the computer is connected to the peripheral equipment.

When control pulse NISQ is applied to the set side of the NISQL flip-flop (figure 4-128), the NISQL flip-flop will set, provided signal STRTFC is not present. Control pulse NISQ is produced during time period T02 or T08 depending on the subinstruction which produces the control pulse. Once the NISQL flip-flop is set, it remains set until signal INKBT1 or STRTFC is produced. Signal INKBT1 occurs at time period T01 when

no counter incrementing is in progress as indicated by the absence of signal INKL. Signal STRTFC may occur anytime during an MCT if produced by signal GOJAM or at a time period predetermined by the peripheral equipment if produced by signal MTCSAI.

Signals CSQG, RBSQ, and WSQG are produced during time period T12 provided that the NISQL flip-flop is set and signal RPTFRC is not present. The clear, read, and write signals are phased by the clear timing signal CT, the read timing signal RT, and the write timing signal WT, respectively. When the start or transfer control to specified address instruction is to be executed, the NISQL flip-flop is reset and signals RBSQ and WSQG are inhibited. However, signal CSQG is produced by signal STRTFC and forces the SQ register to the 0 000 000 state. If signal RPTFRC is present, signals CSQG, RBSQ, and WSQG are not produced. Signal RPTFRC is applied to register SQ and forces it to the 1 000 111 state.

The priority control supplies signal RUPTOR to the register SQ control when the interrupt instruction is to be executed. Signal RUPTOR may be inhibited in the register SQ control by several conditions, one of which is the programmed interrupt inhibit called INHINT. The INHINT condition is established by executing instruction INHINT whose order code is 00.0004. This instruction produces signal INHPLS which is applied to the set side of the INHINT flip-flop (figure 4-128). The INHINT flip-flop will set provided signal GOJAM is not present at the application of signal INHPLS. Once the flip-flop is set, it remains set until signal GOJAM or RELPLS is produced. Signal RELPLS is produced by instruction RELINT which releases the interrupt inhibit condition. Instruction RELINT has the order code 00.0003. Signal MINHL from the INHINT flip-flop is connected to an indicator on the peripheral equipment. This indicator lights when the INHINT flip-flop is set.

Another condition which inhibits signal RUPTOR is the interrupt in progress (IIP) condition. The IIP condition is established during the execution of the interrupt instruction to indicate that an interrupt is in progress. Subinstruction RUPT0 produces signal 9XP1 which is applied to the set side of the IIP flip-flop (figure 4-128). The IIP flip-flop will set provided signal GOJAM is not present at the application of signal 9XP1. Signal 9XP1 is an action or crosspoint pulse produced during time period T09 of subinstruction RUPT0. Once the IIP flip-flop is set, it remains set until signal GOJAM or 5XP4 is produced. Signal 5XP4 is produced by subinstruction RSM3 which is executed at the completion of an interrupt sequence. Subinstruction RSM3 is part of the RESUME instruction (order code 05.0017) which returns control to the program that was being executed before the interrupt occurred. Signal 5XP4 is also an action or crosspoint pulse which is produced during time period T05. Signal MIIP from the IIP flip-flop is connected to the peripheral equipment. A switch on the peripheral equipment will permit signal MIIP to light an indicator and to cause a monitor T12 stop. This causes the time pulse generator (which produces signals T01 through T12) to stop at time period T12 until it is released by the peripheral equipment. The peripheral equipment can supply signal MNHRPT to the register SQ control. This signal is produced by a switch closure and inhibits signal RUPTOR.

REGISTER SQ CONTROL	
SIGNAL	EQUATION
NISQL	$\mathrm{NISQ}\ \overline{\mathrm{STRTFC}} + \overline{\mathrm{INKBT1}}\ \overline{\mathrm{STRTFC}}\ \mathrm{NISQL}$
INKBT1	$\overline{\mathrm{INKL}}\ \mathrm{T01}$
STRTFC	$\mathrm{GOJAM} + \mathrm{MTCSAI}$
CSQG	$(\mathrm{NISQL}\ \overline{\mathrm{RPTFRC}} + \mathrm{STRTFC})\ \mathrm{T12}\ \mathrm{CT}$
RBSQ	$\mathrm{NISQL}\ \overline{\mathrm{RPTFRC}}\ \mathrm{T12}\ \mathrm{RT}$
WSQG	$\mathrm{NISQL}\ \overline{\mathrm{RPTFRC}}\ \mathrm{T12}\ \mathrm{WT}$
INHINT	$\mathrm{INHPLS}\ \overline{\mathrm{GOJAM}} + \mathrm{INHINT}\ \overline{\mathrm{RELPLS}}\ \overline{\mathrm{GOJAM}}$
IIP	$\mathrm{9XP1}\ \overline{\mathrm{GOJAM}} + \mathrm{IIP}\ \overline{\mathrm{5XP4}}\ \overline{\mathrm{GOJAM}}$
RPTFRC	$\mathrm{RUPTOR}\ \mathrm{NISQL}\ \mathrm{T12}\ \mathrm{PHS2}\ \overline{\mathrm{INHINT}}\ \overline{\mathrm{IIP}}\ \overline{\mathrm{MNHRPT}}$ $\overline{\mathrm{FUTEXT}}\ \overline{\mathrm{STRTFC}} + \overline{\mathrm{STRTFC}}\ \overline{\mathrm{T02}}\ \mathrm{RPTFRC}$

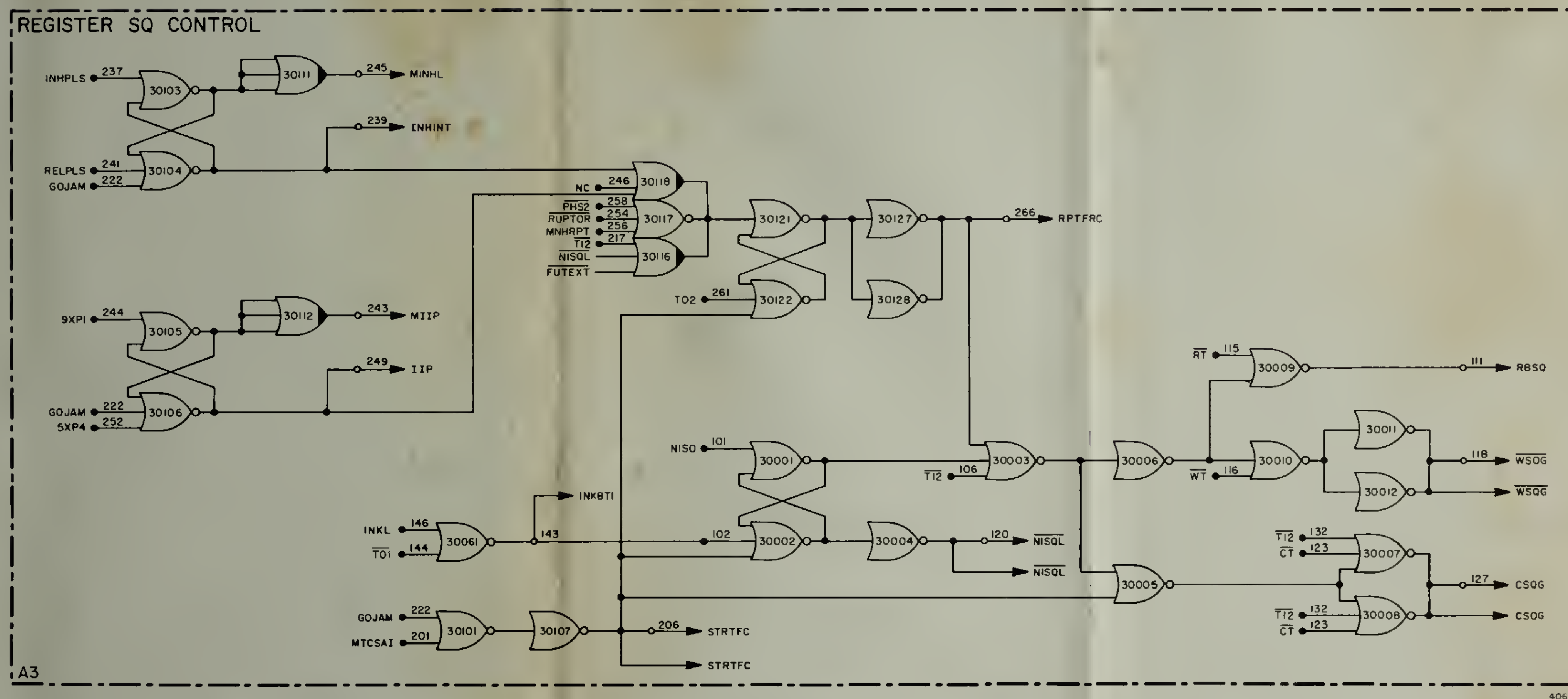


Figure 4-128. Register SQ Control, Logic Diagram

Signal FUTEXT is produced by the register SQ and decoder circuits. This signal is present when the next instruction to be executed is an extracode instruction. Signal FUTEXT is produced when instruction EXTEND or NDX is executed and occurs at time period T08 or T10, respectively. Signal RUPTOR is inhibited by the future extend condition because this condition cannot be re-established when returning to the interrupted program through instruction RESUME. The order codes for instructions EXTEND and NDX which establish the future extend condition are 00.0006 and 15, respectively.

Signal RUPTOR will cause the RPTFRC flip-flop to set at time period T12 subject to the phasing of signal PHS2. A new instruction must be in the process of being called in order for the RPTFRC flip-flop to set. This condition is established by signal NISQL. The RPTFRC flip-flop will set only if signal STRTFC is not present at the same time the set signal is present. The flip-flop is reset at time period T02 or when signal GOJAM or MTCSAI is present.

4-5.4.5 Register SQ and Decoders. Register SQ is a seven-bit register which stores the content of the extended order code field as each instruction is being executed. The content of register SQ and decoders produces signals SQEXT, SQ0 through SQ7, QC0 through QC3, and SQR10. These signals are used by the command generator to produce subinstruction and instruction commands.

Register SQ (figure 4-129) is connected to the central processor by write line signals WL16 and WL14 through WL10. The register SQ control produces signal RBSQ which places the order code content of register B onto the write lines. It also produces signal CSQG which clears register SQ and WSQG which writes the new order code into register SQ. Signal CSQG does not clear the SQEXT bit position. This bit position is set when an extracode instruction is to be executed and is controlled by the FUTEXT flip-flop.

Special purpose control pulses EXTPLS and EXT are applied to the set side of the FUTEXT flip-flop. The flip-flop will set provided signal STRTFC is not present at the application of signals EXTPLS or EXT. Signal EXTPLS is produced at time pulse T08 by instruction EXTEND. The order code for the EXTEND instruction is 00.0006. Signal EXT is produced at time pulse T10 of subinstruction NDXX1. The FUTEXT flip-flop remains set until signal INKBT1 or STRTFC is produced. Signal INKBT1 occurs at time pulse T01 when no counter incrementing is in progress.

The SQEXT flip-flop can be set at time pulse T12 provided the NISQL and the FUTEXT flip-flops are set. If signal STRTFC is present, the NISQL and FUTEXT flip-flops will be reset and their outputs will cause the SQEXT flip-flop to reset also. Signal RPTFRC also sets the SQEXT flip-flop provided a new instruction is being called and signal STRTFC is not present. Once the SQEXT flip-flop is set, it remains set until the next basic instruction is executed. The resetting of the SQEXT flip-flop is accomplished when signal FUTEXT is not present and signals NISQL and T12 are.

When the start or transfer control to specified address instruction is to be executed, signal STRTFC resets the SQEXT flip-flop as specified in the preceeding paragraph. It

also produces signal CSQG which clears bit positions 16 and 14 through 10 of register SQ. As a result, register SQ is forced to the 0 000 000 state which causes the execution of instruction GOJ or TCSA depending on the state of the stage counter. When the interrupt instruction is to be executed, signal RPTFRC sets bit positions SQEXT and 12 through 10 and resets bit positions 10, 14, and 13 of register SQ. As a result, register SQ is forced to the 1 000 111 state which causes the execution of instruction RUPT.

Signals MSQEXT, MSQ16, and MSQ14 through MSQ10 are connected to indicators on the peripheral equipment so that the content of register SQ can be monitored at any time.

The SQ decoder produces signals SQ0 through SQ7 from the outputs of bit positions 16, 14, and 13 of register SQ. These signals are used in the command generator together with signals SQEXT, QC0 through QC3, and SQR10 to produce subinstruction and instruction commands. Signals SQ0 through SQ7 are inhibited by signal INKL. Signal INKL is produced when a counter instruction is being executed. When signal INKL is present, no commands can be produced other than those for the counter and peripheral instructions.

The QC decoder produces signals QC0 and QC3 for the outputs of bit positions 12 and 11 of register SQ. These signals are also used to produce subinstruction and instruction commands and are not inhibited by counter incrementing.

4-5.4.6 Stage Counter and Decoder. The stage counter and decoder (figure 4-130) is regulated by special purpose control pulses ST1, ST2, DVST, RSTSTG, and TRSM from the control pulse generator and by order code signals GOJAM and MTCSAI from the priority control and peripheral equipment, respectively. The stage counter is used as a storage device which is forced to a different state after the execution of each subinstruction. The stage counter remains in a given state for one MCT, the duration of every subinstruction. The stage counter is forced through various counts depending on the instruction being executed. Most instructions are two MCT's long and are completed by executing subinstruction STD2. As a result, the stage counter is advanced through states 000 and 010. Some instructions are three MCT's long and are completed by executing subinstruction STD2. The stage counter states for these instructions are 000, 001, and 010. Other combinations of states are simply 000 for the transfer control instruction, 000 and 001 for the index instructions, 000 and 011 for the RESUME instruction, and 000, 001, and 011 for the multiply instruction. The divide instruction is seven MCT's long. Gray code counts 000, 001, 011, 111, 110, and 100 are used to enumerate six MCT's of this instruction. The seventh MCT is controlled by state 010 which is that of subinstruction STD2.

The stage counter contains three primary level flip-flops A, B, and C, and three secondary level flip-flops STG1, STG2, and STG3, respectively. The secondary level flip-flops are set to the state of the primary level flip-flops at time pulse T12 for most instructions. For the divide instruction, the transfer of states occurs at time pulses T03 and T12. The primary level flip-flops are reset at time pulse T01 to establish the state 000.

REGISTER SQ

SIGNAL	EQUATION
FUTEXT	(EXTPLS + EXT) $\overline{\text{STRTFC}}$ + $\overline{\text{INKBTI}}$ $\overline{\text{STRTFC}}$ FUTEXT
SQEXT	FUTEXT NISQ T12 + RPTFRC $\overline{\text{NISQL T12}}$ $\overline{\text{STRTFC}}$ + SQEXT · (FUTEXT + $\overline{\text{NISQL T12}}$ $\overline{\text{STRTFC}}$)
SQR16	WL16 WSQC $\overline{\text{CSQC}}$ + SQR16 $\overline{\text{CSQG}}$ $\overline{\text{RPTFRC}}$
SQR14	WL14 WSQC $\overline{\text{CSQG}}$ + SQR14 $\overline{\text{CSQG}}$ $\overline{\text{RPTFRC}}$
SQR13	WL13 WSQC $\overline{\text{CSQG}}$ + SQR13 $\overline{\text{CSQG}}$ $\overline{\text{RPTFRC}}$
SQR12	WL12 WSQG $\overline{\text{CSQG}}$ + RPTFRC + SQR12 $\overline{\text{CSQG}}$
SQR11	WL11 WSQG $\overline{\text{CSQC}}$ + RPTFRC + SQR11 $\overline{\text{CSQG}}$
SQR10	WL10 WSQC $\overline{\text{CSQG}}$ + RPTFRC + SQR11 $\overline{\text{CSQG}}$

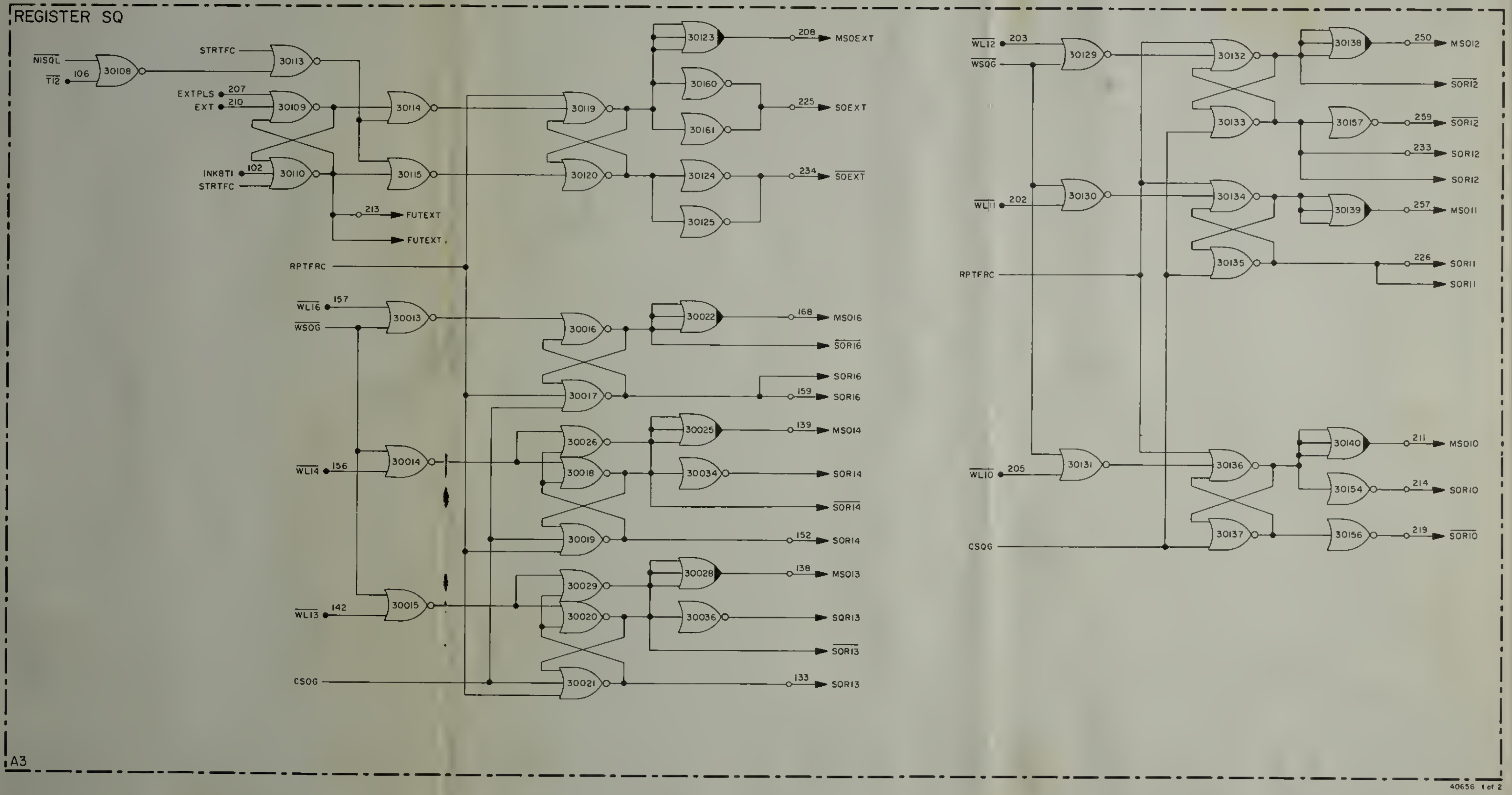
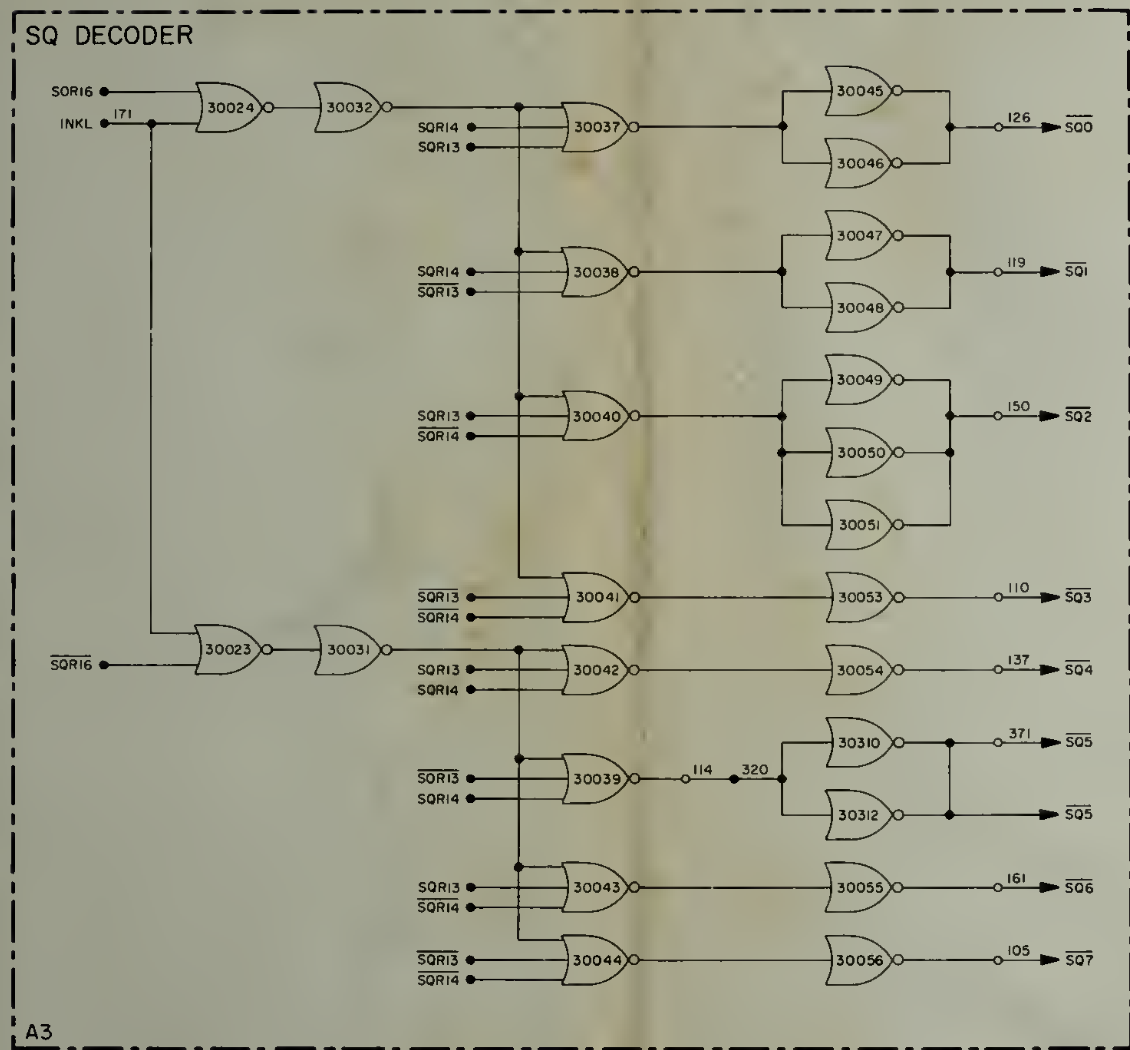
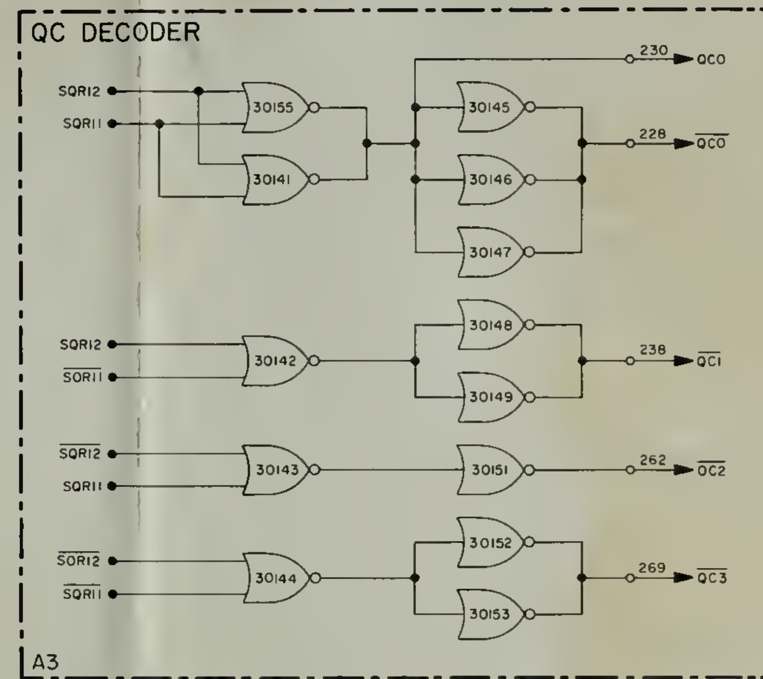


Figure 4-129. Register SQ and Decoder, Logic Diagram (Sheet 1 of 2)





SQ DECODER	
SIGNAL	EQUATION
SQ0	$\overline{SQR16}$ $\overline{SQR14}$ $\overline{SQR13}$ $\overline{INKL}$
SQ1	$\overline{SQR16}$ $\overline{SQR14}$ SQR13 $\overline{INKL}$
SQ2	$\overline{SQR16}$ SQR14 $\overline{SQR13}$ $\overline{INKL}$
SQ3	$\overline{SQR16}$ SQR14 SQR13 $\overline{INKL}$
SQ4	SQR16 $\overline{SQR14}$ $\overline{SQR13}$ $\overline{INKL}$
SQ5	SQR16 $\overline{SQR14}$ SQR13 $\overline{INKL}$
SQ6	SQR16 SQR14 $\overline{SQR13}$ $\overline{INKL}$
SQ7	SQR16 SQR14 SQR13 $\overline{INKL}$

QC DECODER	
SIGNAL	EQUATION
QC0	$\overline{SQR12}$ $\overline{SQR11}$
QC1	$\overline{SQR12}$ SQR11
QC2	SQR12 $\overline{SQR11}$
QC3	SQR12 SQR11

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Figure 4-129. Register SQ and Decoder, Logic Diagram (Sheet 2 of 2)

STAGE COUNTER	
SIGNAL	EQUATION
A	$ST1 + (GOJAM + MTCSA1)\;\overline{T01} + OVST\;\overline{STG3} + A\;\overline{T01}$
B	$ST2\;\overline{GOJAM} + MTCSA1\;\overline{T01} + OVST\;STG1\;\overline{GOJAM} + NOR100\;X87\;XT1\;TRSM\;\overline{GOJAM}\;\overline{T01} + B\;\overline{T01}\;GOJAM$
C	$OVST\;STG2\;\overline{STRTFC} + C\;\overline{T01}\;\overline{STRTFC}$
T12USE	$OVST\;\overline{GOJAM} + T12USE\;\overline{GOJAM}\;\overline{RSTSTG}$
D	$T12\;\overline{T12USE}\;PHS3 + T03\;T12USE\;PHS3$
STG1	$A\;D + STG1\,(A + \bar{D})$
STG2	$B\;D + STG2\,(B + \bar{D})$
STG3	$C\;D + STG3\,(C + \bar{D})$

STAGE DECODER	
SIGNAL	EQUATION
ST0	$\overline{STG3}\;\overline{STG2}\;\overline{STG1}$
ST02	$\overline{STG3}\;STG2\;\overline{STG1}\;\overline{INKL}$
ST3	$\overline{STG3}\;STG2\;STG1$
ST10	$\overline{STG3}\;\overline{STG2}\;STG1$
ST1376	$ST10 + ST376$
ST376	$STG2\,(STG1 + STG3)$
ST3764	$ST376 + ST4$
ST4	$STG3\;\overline{STG2}\;\overline{STG1}$

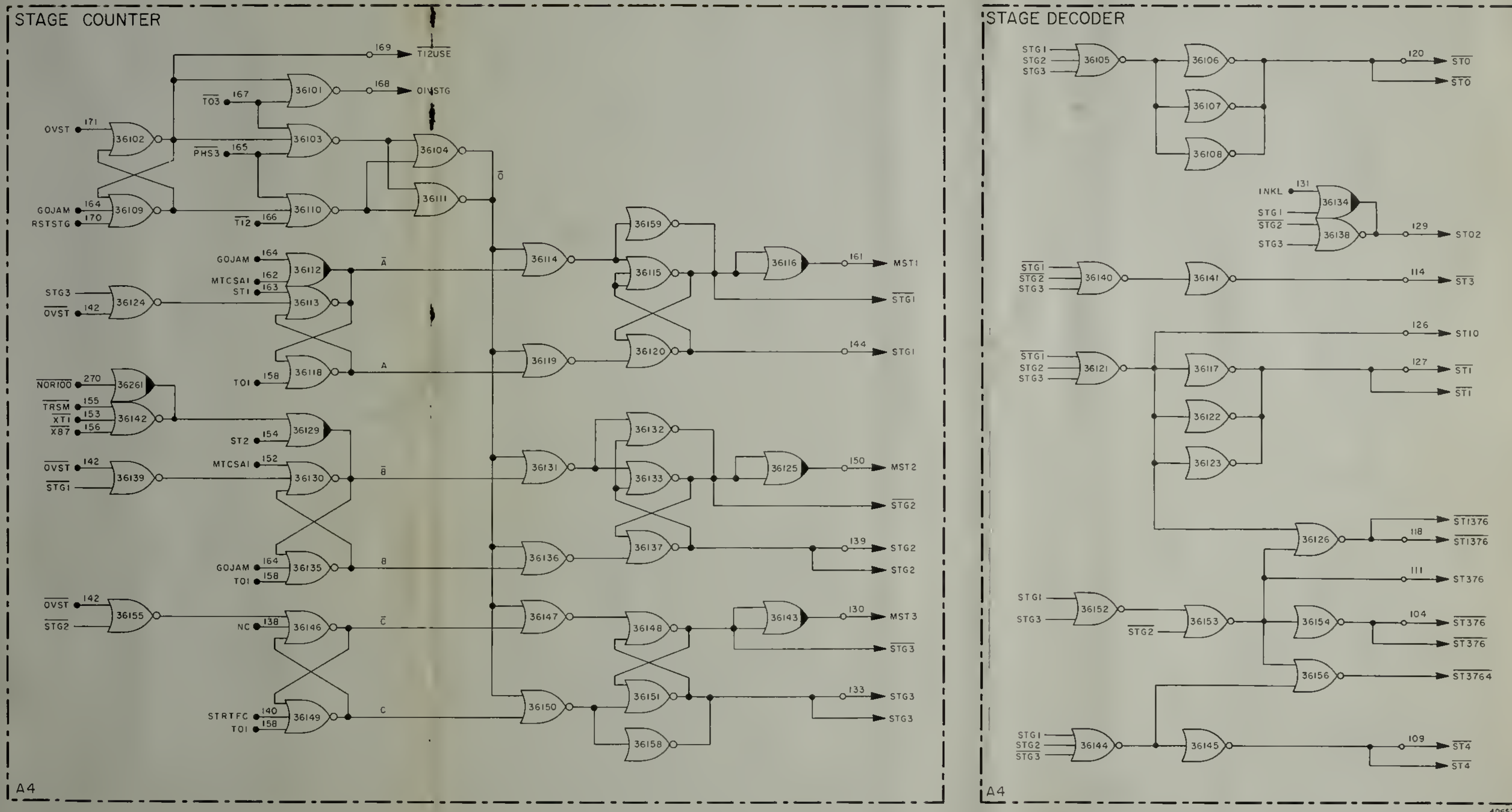

Figure 4-130. Stage Counter and Decoder, Logic Diagram

The stage counter can establish state 001 three ways. When the start instruction is to be executed, signal GOJAM sets flip-flop A and resets flip-flop B. Flip-flop C is reset by signal STRTFC. Control pulse ST1 sets flip-flop A (at time pulse T10) and control pulse DVST sets the flip-flop (at time pulse T02) provided that flip-flop STG3 is not set during the Gray code count sequence.

The state 010 can only be produced in one way, by control pulse ST2 which sets flip-flop B at time pulse T08 or T10 depending on the subinstruction which produces the control pulse.

The state 011 can be produced four ways. When the transfer control to specified address instruction is to be executed, signal MTCSAI sets flip-flops A and B and signal STRTFC resets flip-flop C. During the execution of subinstruction MP1, control pulses ST1 and ST2 are produced at time pulse T10. These control pulses set flip-flops A and B and cause the execution of subinstruction MP3. During the execution of instruction RESUME, control pulse TRSM sets flip-flop B at time pulse T05. Instruction RESUME is an address-dependent instruction consisting of subinstructions NDX0 and RSM3. The content of register S must be octal 0017 for control pulse TRSM to set flip-flop B. At time pulse T10 of subinstruction NDX0, control pulse ST1 sets flip-flop A thereby establishing the state 011 for subinstruction RSM3. During the execution of the divide instruction, control pulse DVST sets flip-flop A at time pulse T02 provided that flip-flop STG3 is not set. Flip-flop B is set by DVST provided flip-flop STG1 is set. Since flip-flop STG2 is not set when control pulse DVST is produced, flip-flop C remains reset, thus establishing state 011.

States 111, 110, and 100 are established by control pulse DVST at time pulse T02 of instruction divide. Flip-flops A, B, and C are set provided that flip-flop STG3 is not set and flip-flops STG1 and STG2 are set, respectively. This establishes state 111. States 110 and 100 are established in a similar way and are dependent on the states of flip-flops STG1, STG2, and STG3.

The contents of flip-flops A, B, and C are transferred to flip-flops STG1, STG2, and STG3, respectively, at time pulse T12 if the T12USE flip-flop is not set. The transfer is subject to the phasing of signal PHS3. The T12USE flip-flop is set at time pulse T02 by control pulse DVST provided signal GOJAM is not present. Once the flip-flop is set, it remains set until reset by control pulse RSTSTG (which occurs at time pulse T08 of subinstruction DV4) unless signal GOJAM occurs first. When the T12USE flip-flop is set, the contents of the primary level flip-flops are transferred to the secondary level flip-flops at time pulse T03 according to the phase of signal PHS3. Signal DIVSTG is also produced at time pulse T03 under these conditions. When the secondary level flip-flops are set, they cannot be reset unless signal D is present. Signals MST1, MST2, and MST3 are connected to lights on the peripheral equipment to indicate the state of the stage counter.

The stage decoder (figure 4-130) produces signals ST0, ST1D, STD2, ST3, ST4, ST1376, ST376, and ST3764. This signal group is the decoded output of the stage counter

and is used in conjunction with signals SQEXT, SQ0 through SQ7, QC0 through QC3, and SQR10 to produce subinstruction and instruction commands. Signals ST0, ST1D, STD2, ST3 and ST4 are produced when the stage counter is set to states 000, 001, 010, 011, and 100, respectively. Signal ST376 is produced when the stage counter is in state 011, 111, or 110. Likewise, signal ST1376 is produced when the stage counter is set to state 001, 011, 111, or 110, and signal ST3764 is produced during states 011, 111, 110, or 100.

4-5.4.7 Subinstruction Decoder. The subinstruction decoder receives the SQ and ST code signals from the order code processors and produces signals called subinstruction and instruction commands. Signals SQEXT, SQ0 through SQ7, QC0 through QC3, and SQR10 comprise the SQ code signals. Signals ST0 through ST4, ST376, ST1376, and ST3764 comprise the ST code signals. The SQEXT and SQR10 signals represent the high and low order bits, respectively, of register SQ. Signals SQ0 through SQ7 represent octal quantities 0 through 7 respectively, in bit positions 16, 14, and 13 of register SQ. Signals QC0 through QC3 represent octal quantities 0 through 3, respectively, in bit positions 12 and 11 of register SQ. The SQ and QC signals are the decoded outputs of the register SQ and decoder circuits. The ST code signals represent the state of the stage counter. For example, signal ST1 represents state 001. The ST signals are the decoded outputs of the stage counter and decoder circuits.

The subinstruction decoder utilizes the SQ and ST code signals in producing subinstruction and instruction commands. The command signals in turn are ANDed with time pulses T01 through T12 as necessary to produce crosspoint signals. This action is accomplished in the crosspoint generator. The crosspoint signals produce the control pulses which regulate the data flow of the computer. By definition, a subinstruction command is used for only one subinstruction. For example, command STD2 is used only during subinstruction STD2. An instruction command is therefore defined as a command which is used by two or more subinstructions. For example, command IC3 is used for subinstructions STD2, TC0, and TCF0. Table 4-IX lists all of the commands produced by the various SQ and ST codes. The subinstructions which relate to the specific SQ and ST codes are also listed in table 4-IX.

Figure 4-131 shows the logic circuits that produce the subinstruction commands for basic, channel, and extracode instructions. Signal CCS0 is used as an example to illustrate the production of commands. When subinstruction CCS0 is to be executed, register SQ is set to the 0 001 00X state and the stage counter is set to 000. As a result, the order code processor supplies signals SQ1, QC0, and ST0 to the command generator. Since CCS is a basic instruction, the high order bit of register SQ is a logic ZERO and signal SQEXT is not present. The circuit for basic instructions detects this condition and produces signal NEXST0. Had signal ST1 been present instead of ST0, signal NEXST0 would not be produced. Signals NEXST0, SQ1, and QC0 are then ANDed to produce subinstruction command CCS0.

The QC signals are produced by the two high order bits of the address field. Instructions which do not use the extended order code field have commands that are produced

Table 4-IX. Commands Per Subinstruction

Subinstruction	SQ Code	ST Code	BR1 and BR2	Commands
BASIC INSTRUCTIONS				
STD2		2		STD2 IC3
TC0	00	0		TC0 IC3
CCS0	010	0		CCS0 IC12
TCF0	011- 013	0		TCF0 IC3
DAS0	020	0		DAS0 IC10
DAS1	020	1		DAS1
LXCH0	021	0		IC8 IC9
INCR0	022	0		INCR0 PRINC
ADS0	023	0		ADS0 DAS1
CA0	03	0		IC6 IC13
CS0	04	0		IC7 IC13
NDX0	050	0		NDX0 IC1 IC13
NDX1	050	1		IC2
RSM3	050	3		RSM3

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Table 4-IX. Commands Per Subinstruction

Subinstruction	SQ Code	ST Code	BR1 and BR2	Commands
BASIC INSTRUCTIONS (cont)				
DXCH0	051	0		DXCH0 IC8 IC10
DXCH1	051	1		IC5 IC9
TS0	052	0		TS0 IC9
XCH0	053	0		IC5 IC9
AD0	06	0		AD0 IC11 IC13
MASK0	07	0		MASK0 IC14
EXTRACODE INSTRUCTIONS				
DV0	110	0		DV0 DIV
DV1	110	1		DV1 DV1376 DIV
DV3	110	3		DV1376 DV376 DIV
DV7	110	7		DV1376 DV376 DIV

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Table 4-IX. Commands Per Subinstruction

Subinstruction	SQ Code	ST Code	BR1 and BR2	Commands
EXTRACODE INSTRUCTIONS (cont)				
DV6	110	6		DV1376 DV376 DIV
DV4	110	4		DV4
BZF0	111- 113	0	XX X0 X1	IC15 IC17 IC16
MSU0	120	0		MSU0 IC12
QXCH0	121	0		QXCH0 IC9
AUG0	122	0		AUG0 PRINC
DIM0	123	0		DIM0 PRINC
DCA0	13	0		DCA0 IC4 IC10 IC13
DCA1	13	1		IC6 IC13
DCS0	14	0		DCS0 IC4 IC10 IC13
DCS1	14	1		IC7 IC13

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Table 4-IX. . Commands Per Subinstruction

Subinstruction	SQ Code	ST Code	BR1 and BR2	Commands
EXTRACODE INSTRUCTIONS (cont)				
NDXX0	15	0		IC1 IC13
NDXX1	15	1		NDXX1 IC2
SU0	160	0		SU0 IC11 IC13
BZMF0	161- 163	0	XX 00 X1 1X	IC15 IC17 IC16 IC16
MP0	17	0		MP0 IC14
MP1	17	1		MP1
MP3	17	3		MP3
CHANNEL INSTRUCTIONS				
READ0	1000	0		READ0 INOUT
WRITE0	1001	0		WRITE0 INOUT
RAND0	1010	0		RAND0 INOUT
WAND0	1011	0		WAND0 INOUT
ROR0	1020	0		ROR0 INOUT

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Table 4-IX. Commands Per Subinstruction

Subinstruction	SQ Code	ST Code	BR1 and BR2	Commands
CHANNEL INSTRUCTIONS (cont)				
WOR0	1021	0		WOR0 INOUT
RXOR0	1030	0		RXOR0 INOUT IC14
INTERRUPT INSTRUCTIONS				
RUPT0	1031	0		RUPT0
RUPT1	1031	1		RUPT1
GOJ1	00	1		GOJ1
COUNTER INSTRUCTIONS				
PINC				PINC PARTC INKL
MINC				MINC PARTC INKL
PCDU				PCDU PARTC INKL
MCDU				MCDU PARTC INKL
DINC				DINC PARTC INKL
SHINC				SHIFT INKL
SHANC				SHANC SHIFT INKL

(Sheet 5 of 6)

Table 4-IX. Commands Per Subinstruction

Subinstruction	SQ Code	ST Code	BR1 and BR2	Commands
PERIPHERAL INSTRUCTIONS				
TCSAJ3	00	3		TCSAJ3
INOTRD				CHINC INKL MON+CH
INOTLD				INOTLD CHINC INKL MON+CH
FETCH0		0		FETCH0 MON INKL MON+CH
FETCH1		1		MON STFET1 INKL MON+CH
STORE0		0		FETCH0 MON INKL MON+CH
STORE1		1		MON STFET1 STORE1 INKL MON+CH

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BASIC INSTRUCTIONS	
SIGNAL	EQUATION
TCO	$\overline{SQEXT}$ SQ0 ST0
GOJ1	$\overline{SQEXT}$ SQ0 ST1
TCSAJ3	$\overline{SQEXT}$ SQ0 ST3
CCS0	$\overline{SQEXT}$ SQ1 QC0 ST0
TCF0	$\overline{SQEXT}$ SQ1 $\overline{QC0}$ ST0
DAS0	$\overline{SQEXT}$ SQ2 QC0 ST0
DAS1	$\overline{SQEXT}$ SQ2 QC0 ST1 + ADS0
LXCH0	$\overline{SQEXT}$ SQ2 QC1 ST0
INCR0	$\overline{SQEXT}$ SQ2 QC2 ST0
ADS0	$\overline{SQEXT}$ SQ2 QC3 ST0
NDX0	$\overline{SQEXT}$ SQ5 QC0 ST0
RSM3	$\overline{SQEXT}$ SQ5 QC0 ST3
DXCH0	$\overline{SQEXT}$ SQ5 QC1 ST0
TS0	$\overline{SQEXT}$ SQ5 QC2 ST0
AD0	$\overline{SQEXT}$ SQ6 ST0
MSK0	$\overline{SQEXT}$ SQ7 ST0

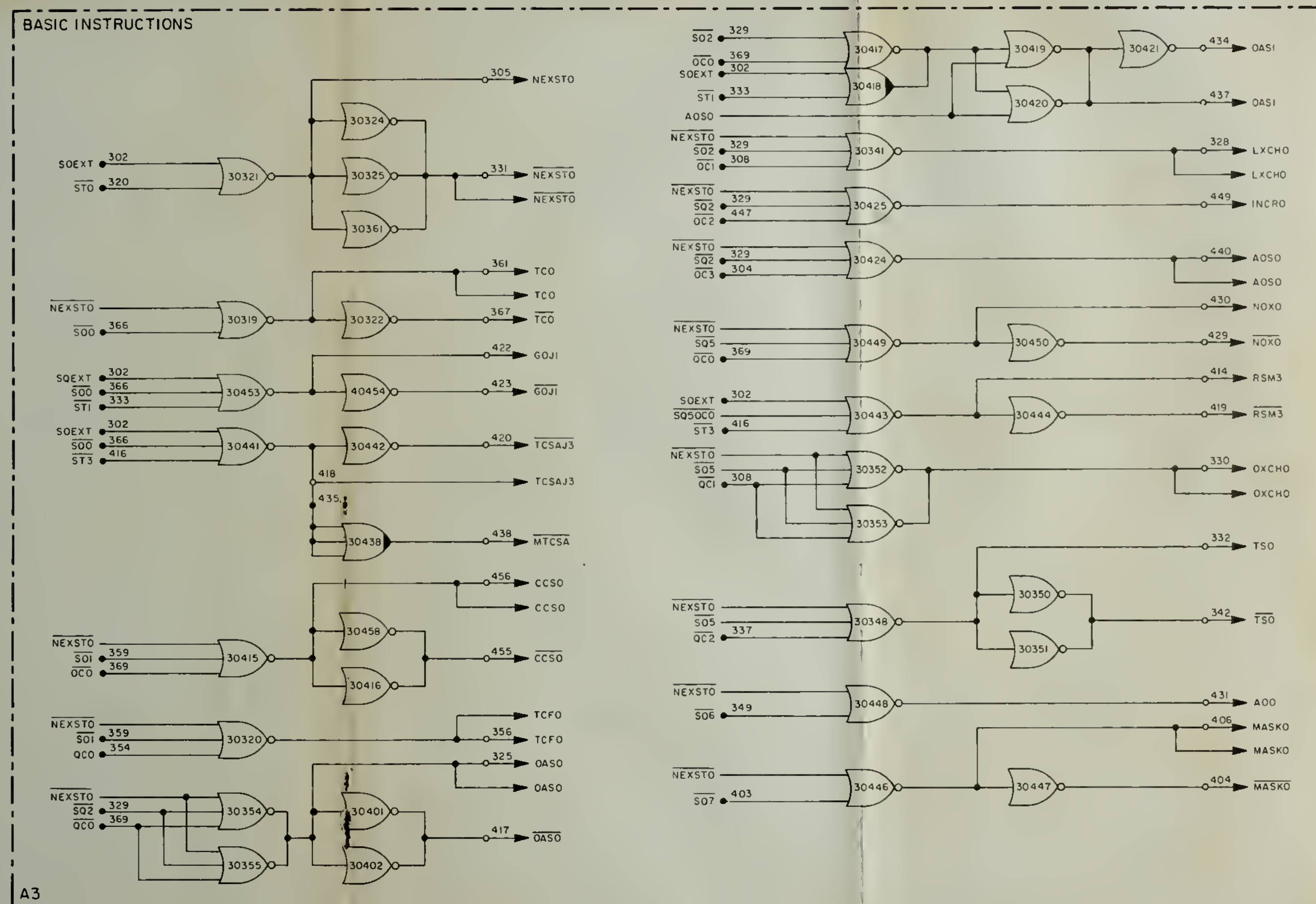

Figure 4-131. Subinstruction Decoder, Logic Diagram (Sheet 1 of 3)

CHANNEL INSTRUCTIONS	
SIGNAL	EQUATION
READ0	SQEXT SQ0 QC0 $\overline{\text{SQR10}}$ ST0
WRITE0	SQEXT SQ0 QC0 SQR10 ST0
RAND0	SQEXT SQ0 QC1 $\overline{\text{SQR10}}$ ST0
WAND0	SQEXT SQ0 QC1 SQR10 ST0
ROR0	SQEXT SQ0 QC2 $\overline{\text{SQR10}}$ ST0
WOR0	SQEXT SQ0 QC2 SQR10 ST0
RXOR0	SQEXT SQ0 QC3 $\overline{\text{SQR10}}$ ST0
RUPT0	SQEXT SQ0 QC3 SQR10 ST0
RUPT1	SQEXT SQ0 QC3 SQR10 ST1

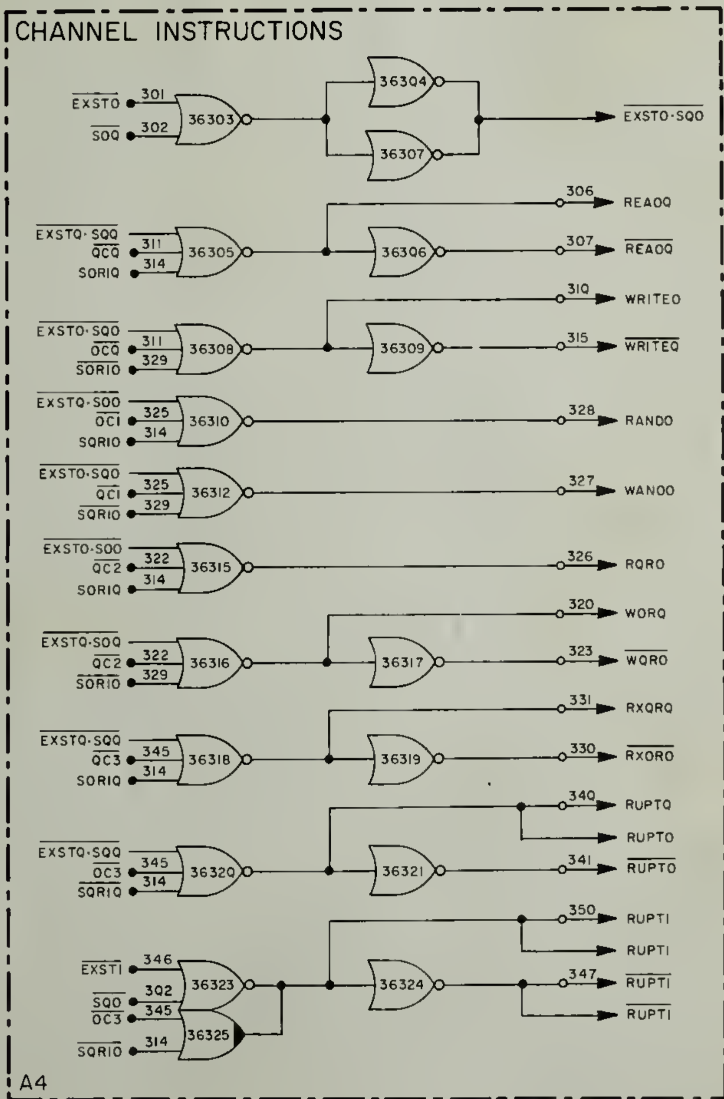

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Figure 4-131. Subinstruction Decoder, Logic Diagram (Sheet 2 of 3)

EXTRACODE INSTRUCTIONS

SIGNAL	EQUATION
DVO	SQEXT SQ1 QCO STO
DVI	SQEXT SQ1 QCO ST1
DV1376	SQEXT SQ1 QCO ST1376
DV376	SQEXT SQ1 QCO ST376
DV3764	SQEXT SQ1 QCO ST3764
DV4	SQEXT SQ1 QCO ST4
BZFO	SQEXT SQ1 $\overline{\text{QCO}}$ STO
MSUO	SQEXT SQ2 QCO STO
QXCHO	SQEXT SQ2 QC1 STO
AUGO	SQEXT SQ2 QC2 STO
DIMO	SQEXT SQ2 QC3 STO
DCAO	SQEXT SQ3 STO
DCSO	SQEXT SQ4 STO
DCSI	SQEXT SQ4 ST1
NDXX1	SQEXT SQ5 ST1
SUO	SQEXT SQ6 QCO STO
BZMFO	SQEXT SQ6 $\overline{\text{QCO}}$ STO
MPO	SQEXT SQ7 STO
MP1	SQEXT SQ7 ST1
MP3	SQEXT SQ7 ST3

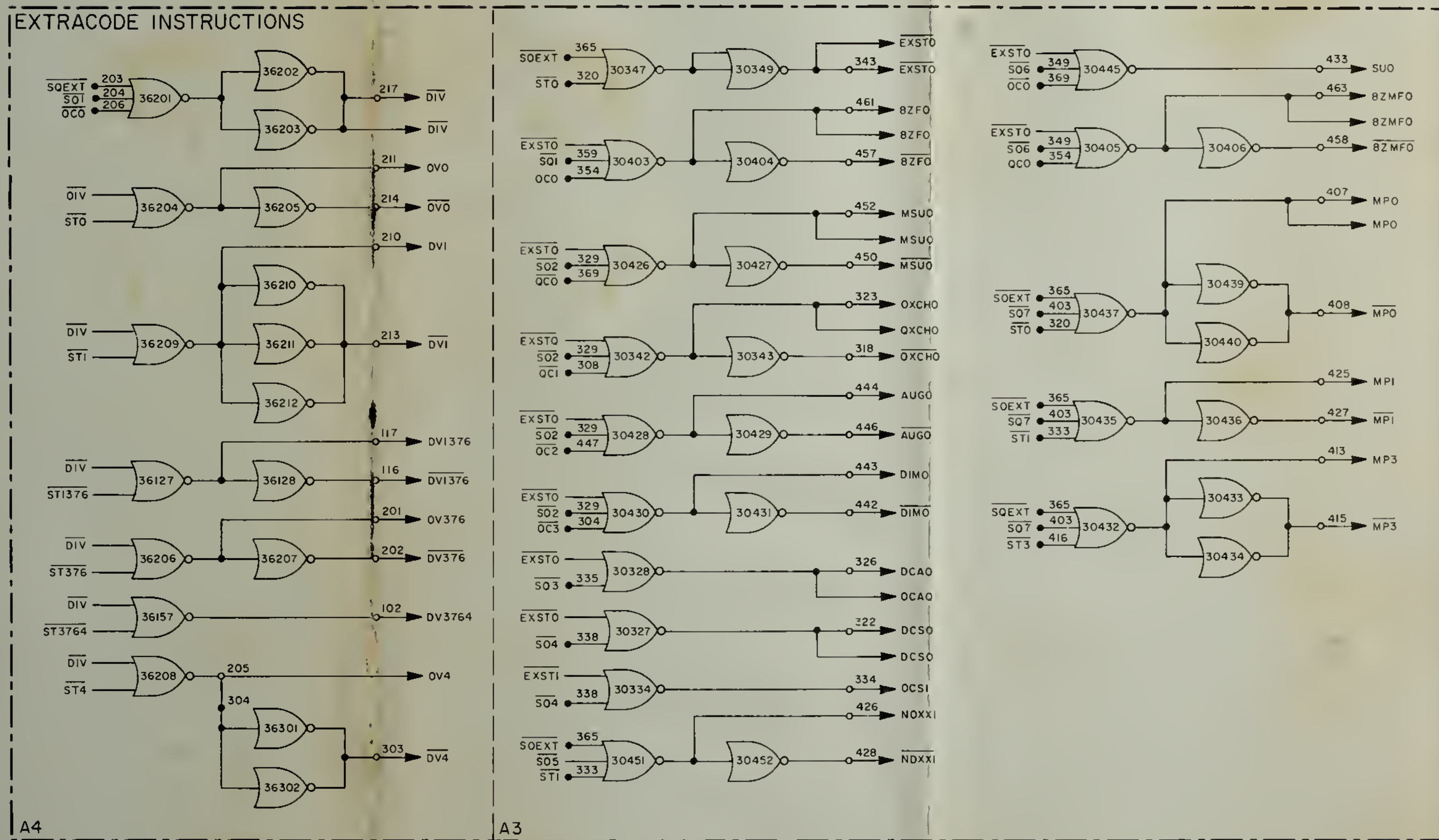

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Figure 4-131. Subinstruction Decoder, Logic Diagram (Sheet 3 of 3)

without the QC signals. The basic instructions which can use any computer address are TC, CA, CS, AD, and MASK. The subinstruction commands produced without QC signals are TC0, AD0, and MASK0. Instructions CA and CS are controlled by instruction command signals from the instruction decoder.

The basic instructions which use the entire order code field are:

(1) CCS	(5) INCR	(9) DXCH
(2) TCF	(6) ADS	(10) TS
(3) DAD	(7) NDX	(11) XCH
(4) LXCH	(8) RESUME	

These instructions have commands which are produced with a QC signal. Other important points concerning basic instructions are that signal DAS1 is an instruction command and signal LXCH0 is not used to produce crosspoint pulses.

Signal DAS1 is an instruction command because it is used for subinstructions DAS1 and ADS0. Subinstruction LXCH0 is controlled by instruction commands IC8 and IC9 which are produced by signal LXCH0. The logic diagram for basic instructions contains the circuits which produce commands TCSAJ3 and GOJ1. These commands are for peripheral and interrupt instructions, respectively, and are included here because they have order codes similar to basic instructions. Signal MTCSA is fed to the peripheral equipment.

The channel instructions and RUPT instruction are controlled by commands which are produced from the entire order code content of register SQ and the content of the stage counter. For example, when subinstruction WAND0 is to be executed, register SQ is set to the 1 000 011 state and the stage counter is set to 000. As a result, signals SQEXT, SQ0, QC1, and SQR10 are present and ANDed to produce subinstruction command WAND0.

The extracode instructions are also shown in figure 4-131. Special attention is given to the commands for the divide instruction because of the Gray code count used to control the commands. When instruction DV is to be executed, register SQ is set to the 1 001 00X state and the stage counter is set to 000. As a result, signals SQEXT, SQ1, QC0, and ST0 are supplied to the subinstruction decoder. Signals SQEXT, SQ1, and QC0 are ANDed to produce instruction command DIV. In addition, signals DIV and ST0 are ANDed to produce subinstruction command DV0. Since signal DIV is produced without an ST signal, it remains for the duration of the divide instruction. It is also used to produce subinstruction commands DV1 and DV4 and instruction commands DV1376, DV376, and DV3764. Subinstructions DV1, DV3, DV7, and DV6 start at time pulse T04 and end at the following time pulse T03. Instruction command DV1376 produces crosspoint pulse for time pulse T01, T02, and T03 whereas instruction command DV376 produces crosspoint pulses for time pulses T04 through T12. Instruction command DV3764 is not used to produce crosspoint pulses but it does turn off fixed memory timing during four MCT's of the divide instruction.

The remaining commands for the extracode instructions are similar to the commands for the basic instructions. Instructions DCA, DCS, NDXX, and MP do not encroach on the address field for their order codes. As a result, the commands for these instructions do nut use a QC signal. Signals BZF0, DCS1, and BZMF0 are not used to produce crosspoint pulses but are used to produce instruction command signals which control the associated subinstructions.

4-5.4.8 Instruction Decoder. The instruction decoder receives the SQ and ST code signals from the order code processor and commands from the subinstruction decoder. The instruction decoder produces commands that are used for two or more subinstructions. These commands are ANDed with time pulses T01 through T12 as necessary to produce crosspoint pulses. Table 4-IX lists the commands produced for each subinstruction. Table 4-X lists the subinstructions that use a particular command for producing crosspoint pulses.

Table 4-X. Subinstructions Per Command

Command	Subinstructions	Command	Subinstructions
AD0	AD0	DIV	DV0 DV1 DV3 DV7 DV6
ADS0	ADS0	DV0	DV0
AUG0	AUG0	DV1	DV1
CCS0	CCS0	DV4	DV4
CHINC	INOTRD INOTLD	DV376	DV3 DV7 DV6
DAS0	DAS0	DV1376	DV1 DV3 DV7 DV6
DAS1	DAS1 ADS0	DXCH0	DXCH0
DCA0	DCA0		
DCS0	DCS0		
DIM0	DIM0		
DINC	DINC		

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Table 4-X. Subinstructions Per Command

Command	Subinstructions
FETCH0	FETCH0 STORE0
GOJ1	GOJ1
IC1	NDX0 NDXX0
IC2	NDX1 NDXX1
IC3	STD2 TC0 TCF0
IC4	DCA0 DCS0
IC5	DXCH1 XCH0
IC6	CA0 DCA1
IC7	CS0 DCS1
IC8	LXCH0 DXCH0
IC9	LXCH0 DXCH1 TS0 XCH0 QXCH0 DAS0
IC10	DXCH0 DCA0 DCS0
IC11	AD0 SU0 CCS0
IC12	MSU0
IC13	CA0 CS0 NDX0 AD0 DCA0 DCA1 DCS0 DCS1 NDXX0 SU0
IC14	MASK0 MP0 RXOR0
IC15	BZF0 BZMF0
IC16	BZF0 BZMF0
IC17	BZF0 BZMF0
INCR0	INCR0
INKL	PINC MINC PCDU MCDU DINC SHINC SHANC INOTRD INOTLD FETCH0 FETCH1 STORE0 STORE1

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Table 4-X. Subinstructions Per Command

Command	Subinstructions	Command	Subinstructions
INOTLD	INOTLD	PARTC	PINC MINC PCDU MCDU DINC
INOUT	READ0 WRITE0 RAND0 WAND0 ROR0 WOR0 RXOR0	PCDU	PCDU
MASK0	MASK0	PINC	PINC
MCDU	MCDU	PRINC	INCR0 AUG0 DIM0
MINC	MINC	QXCH0	QXCH0
MON	FETCH0 FETCH1 STORE0 STORE1	RAND0	RAND0
MON+CH	INOTRD INOTLD FETCH0 FETCH1 STORE0 STORE1	READ0	READ0
MP0	MP0	ROR0	ROR0
MP1	MP1	RSM3	RSM3
MP3	MP3	RUPT0	RUPT0
MSU0	MSU0	RUPT1	RUPT1
NDX0	NDX0	RXOR0	RXOR0
NDXX1	NDXX1	SHANC	SHANC
		SHIFT	SHINC SHANC
		STD2	STD2
		STFET1	FETCH1 STORE1

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Table 4-X. Subinstructions Per Command

Command	Subinstructions	Command	Subinstructions
STORE1	STORE1	TCSAJ3	TCSAJ3
SU0	SU0	TS0	TS0
TC0	TC0	WAND0	WAND0
TCF0	TCF0	WOR0	WOR0
		WRITE0	WRITE0

(Sheet 4 of 4)

Figure 4-132 shows the logic circuits that produce most of the instruction commands for basic, channel, extracode, counter, and peripheral instructions. Two examples are used to describe how the instruction commands are produced. First, consider signal IC5 which is used for subinstructions DXCH1 and XCH0. When subinstruction DXCH1 is to be executed the order code content of register SQ is 0 101 01X and the stage counter is set to 001. As a result, signals SQ5, QC1, and ST1 are present. Since the high order bit is a logic ZERO, signal SQEXT is not present. These conditions are detected by an AND function and signal IC5 is produced. When subinstruction XCH0 is to be executed signals SQ5, QC3, and ST0 are present and signal SQEXT is not present. These conditions are also detected by an AND function and signal IC5 is produced.

The second way to produce instruction command signals is by ORing various subinstruction commands. For example, signal IC12 is produced by subinstruction command CCS0 or MSU0. Another example is signal IC10 which is produced by subinstruction command DXCH0 or DAS0. It is also produced by instruction command signal IC4. Commands IC16 and IC17 are dependent on branch conditions. Signal IC16 is produced by signals BZF0 and BR2 or by signals BZMF0 and either BR1 or BR2. Signal IC17 is produced when signal IC16 is not present because of improper branch conditions during subinstructions BZF0 and BZMF0.

INSTRUCTION DECODER	
SIGNAL	EQUATION
IC1	SQEXT SQ5 STO + SQ5 QCO STO
IC2	SQEXT SQ5 STI + SQ5 QCO STI
IC3	TCO + TCFO + STD2
IC4	DCAO + DCSO
IC5	$\overline{\text{SQEXT}}$ SQ5 QC1 STI + $\overline{\text{SQEXT}}$ SQ5 QC3 STO
IC6	$\overline{\text{SQEXT}}$ SQ3 STO + SQEXT SQ3 STI
IC7	$\overline{\text{SQEXT}}$ SQ4 STO + SQEXT SQ4 STI
IC8	DXCHO + LXCHO
IC9	IC5 + TSO + LXCHO + QXCHO
IC10	IC4 + DXCHO + DASO
IC11	$\overline{\text{SQEXT}}$ SQ6 STO + SQ6 QCO STO
IC12	CCSO + MSUO
IC13	IC1 + IC6 + IC7 + IC11 + DASO + DCAO
IC14	MPO + RXORO + MASKO
IC15	BZFO + BZMFO
IC16	BZFO BR2 + BZMFO (BR1 + BR2)
IC17	IC15 $\overline{\text{IC16}}$
INOUT	SQEXT SQO STO $\overline{\text{RUPTO}}$
PRINC	SQ2 $\overline{\text{QC3}}$ STO + EXT SQ2 SQR12 STO
PARTC	INKL SHIFT (MON + CH)

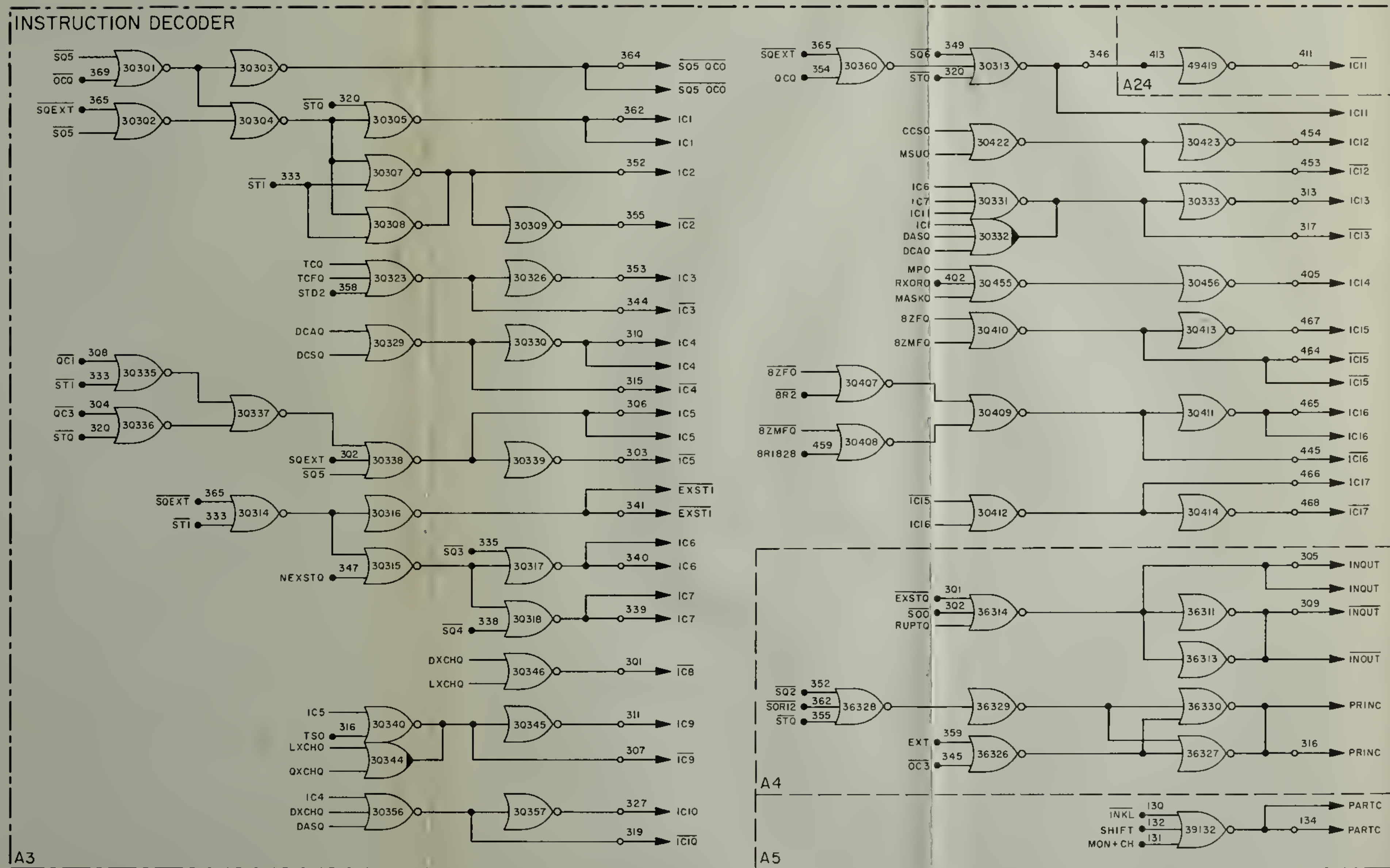

Figure 4-132. Instruction Decoder, Logic Diagram

4-5.4.9 Counter and Peripheral Instruction Control. The counter and peripheral instruction control (figure 4-133) is regulated by signals from the priority control and peripheral equipment. The signals supplied by the priority control are the start order code signal (GOJAM), the counter OR signal (CTROR), and the various counter increment signals that request a particular counter instruction. The prime function of signal GOJAM is to take top priority by inhibiting and resetting many circuits in the counter and peripheral instruction control. Signal CTROR is used to produce the increment signal (INKL) in addition to various strobe signals. The signals supplied by the peripheral equipment are MREAD, MLOAD, MRDCH, MLDCH for FETCH, STORE, INOTRD, and INOTLD instructions, respectively. The peripheral equipment also supplies signal MNHNC for inhibiting the counter increment operation. The counter and peripheral instruction control supplies the following subinstruction commands to the control pulse generator:

(1) STORE1	(4) PCDU	(7) SHANC
(2) PINC	(5) MCDU	(8) DINC
(3) MINC	(6) SHINC	

It also supplies the following instruction commands:

(1) INKL	(3) MONTCH	(5) FETCH0
(2) STFET1	(4) CHINC	

The instruction command signal INKL must always be produced before a counter or peripheral instruction can be executed. Signal INKL interrupts the operation of the register SQ control, SQ decoder, and stage decoder so that no instruction or subinstruction command will be produced while the counter or peripheral instruction is being executed. Signal INKL does not destroy the order code in register SQ; it simply delays recognition of the order code until the counter or peripheral instruction has been executed.

A counter or peripheral instruction cannot be executed if a GOJAM condition exists. Signal GOJAM is applied to the set side of the GNHNC flip-flop. If time pulse T01 is not present, signal GOJAM will set the GNHNC flip-flop. The flip-flop will remain set until the following T01 time pulse. Signal B controls the time at which a counter or peripheral instruction can be executed. Signal B is present at time pulse T12 provided signal NISQL is also present. Signal NISQL is produced by the register SQ control. This signal is present only at the end of each instruction; its absence at time pulse T12 prevents a counter or peripheral instruction from being executed between subinstructions. Signal B is produced during the last quarter interval of time pulse T12 as indicated by the presence of signal PHS4.

When a counter instruction is to be executed, signal CTROR from the priority control is present. The presence of signals B and CTROR will allow a counter increment to occur provided the operation is not manually inhibited by signal MNHNC from the peripheral equipment or by signal A. Signal A is produced whenever a peripheral instruction is to be executed and gives the peripheral instructions priority over the counter instructions. If the preceding conditions are met, flip-flop C will set. The set input to

flip-flop C can be overridden by signal GOJAM if both the set and reset inputs occur at the same time. Signal C will be present for almost a full MCT, starting during the last quarter interval of time pulse T12 and remaining until the third quarter interval of the following T12 pulse. The third quarter reset interval is controlled by signal PHS3. If additional counter incrementing is to take place, the C flip-flop will remain set. It can be reset any time by signal GOJAM or at time pulse T12 if both a counter and a peripheral instruction are requested at the same time. When this happens, signal A in addition to signals T12 and PHS3 will reset the C flip-flop. At the end of all counter incrementing, the absence of signal CTROR will cause the flip-flop to reset at time pulse T12.

Signal INKL is produced directly from signal C or from signal MON+CH which indicates a peripheral instruction is being executed. Signal C also produces signal INCSET at time pulse T02 and signal RSSB during the third quarter of time pulse T07. Signal INCSET causes any counter instruction request to set the associated counter instruction flip-flop. Signal RSSB in conjunction with decoded counter addresses, resets cells in the priority control. This action terminates counter instruction requests applied to the counter and peripheral instructiou control. Signal MINKL is sent to the peripheral equipment and can be used to produce a time pulse T12 stop and turn on an indicator.

Signal A is present when a peripheral instruction is to be executed. The A flip-flop may be set by signal MREAD, MLOAD, MRDCH, or MLDCH from the peripheral equipment. These signals are subjected to the timing of signal PHS2. The flip-flop remains set until the T11 time pulse, during which signal MON+CH is present. The A flip-flop is also reset by signal GOJAM, which may occur at any time.

Signal A resets the C flip-flop at the next T12 time pulse. It is also used to establish a peripheral instruction request. A peripheral instruction cannot be executed before the completion of the current instruction. This action is controlled by signal B which is produced at time pulse T12 when the NISQL flip-flop is set. Signal A is produced by signal MLDCH when the channel load instruction INOTLD is to be executed. Signals MLDCH, A, and B cause the INOTLD flip-flop to set. The channel load instruction is one MCT long. Therefore, the INOTLD flip-flop remains set for one MCT from the last quarter of time pulse T12 as determined by signal B to the second quarter of the following T12 time pulse as determined by reset signals T12 and PHS2. The channel read instruction is controlled by flip-flop INOTRD which is set by signals MRDCH, A, and B and reset by signals T12 and PHS2. The timing of signals INOTLD and INOTRD is identical. These signals are subinstruction commands and either one will produce iustruction commands signals CHINC and MON+CH. Signal MON+CH, in turn, produces signal INKL and also causes the A flip-flop to be reset at time pulse T11.

Instructions STORE and FETCH are both two MCT's long. The STORE flip-flop is set when signals MLOAD, A, and B are all present and signal GOJAM is not present. The STORE flip-flop remains set for two MCT's. During the first MCT, the stage counter is set to the 000 state and produces signal ST0. Signal STORE produces signal MON which in turn is combined with signal ST0 to produce instruction command signal FETCH0. During the second MCT, the stage counter is set to the 001 state and produces signal ST1. Signals STORE and ST1 are then combined to produce subinstruction command

PERIPHERAL INSTRUCTION	
SIGNAL	EQUATION
A	$\overline{(MREAD + MLOAD + MRDCH + MLDCH)\ PHS2}\ \overline{GOJAM} + A\ \overline{GOJAM}\ \overline{T11\ (MON + CH)}$
GNHNC	$GOJAM + GNHNC)\ \overline{T01}$
B	$\overline{GNHNC}\ T12\ NISQL\ PHS4$
C	$\overline{B\ CTROR\ \overline{A}\ \overline{MNHNC}}\ \overline{GOJAM} + C\ \overline{GOJAM}\ \overline{T12\ PHS3\ CTROR\ \overline{A}}$
INCSET	T02 C
RSSB	T07 C PHS3
INKL	C + MON + CH
INOTLO	$MLDCH\ A\ B + INOTLO\ \overline{T12\ PHS2}$
INOTRO	$MDCH\ A\ B + INOTRD\ \overline{T12\ PHS2}$
CHINC	INOTLO + INOTRD
STORE	$\overline{MLOAO\ A\ B}\ \overline{GOJAM} + STORE\ \overline{GOJAM}\ \overline{T12\ PHS2\ MON\ STI}$
STOREI	STORE STI
FETCH	$\overline{MREAD\ A\ B}\ \overline{GOJAM} + FETCH\ \overline{GOJAM}\ \overline{T12\ PHS2\ MON\ STI}$
FETCHI	FETCH STI
STFETI	STOREI + FETCHI
MON	STORE + FETCH
FETCHO	MON STO
MON + CH	STORE + FETCH + INOTLD + INOTRO

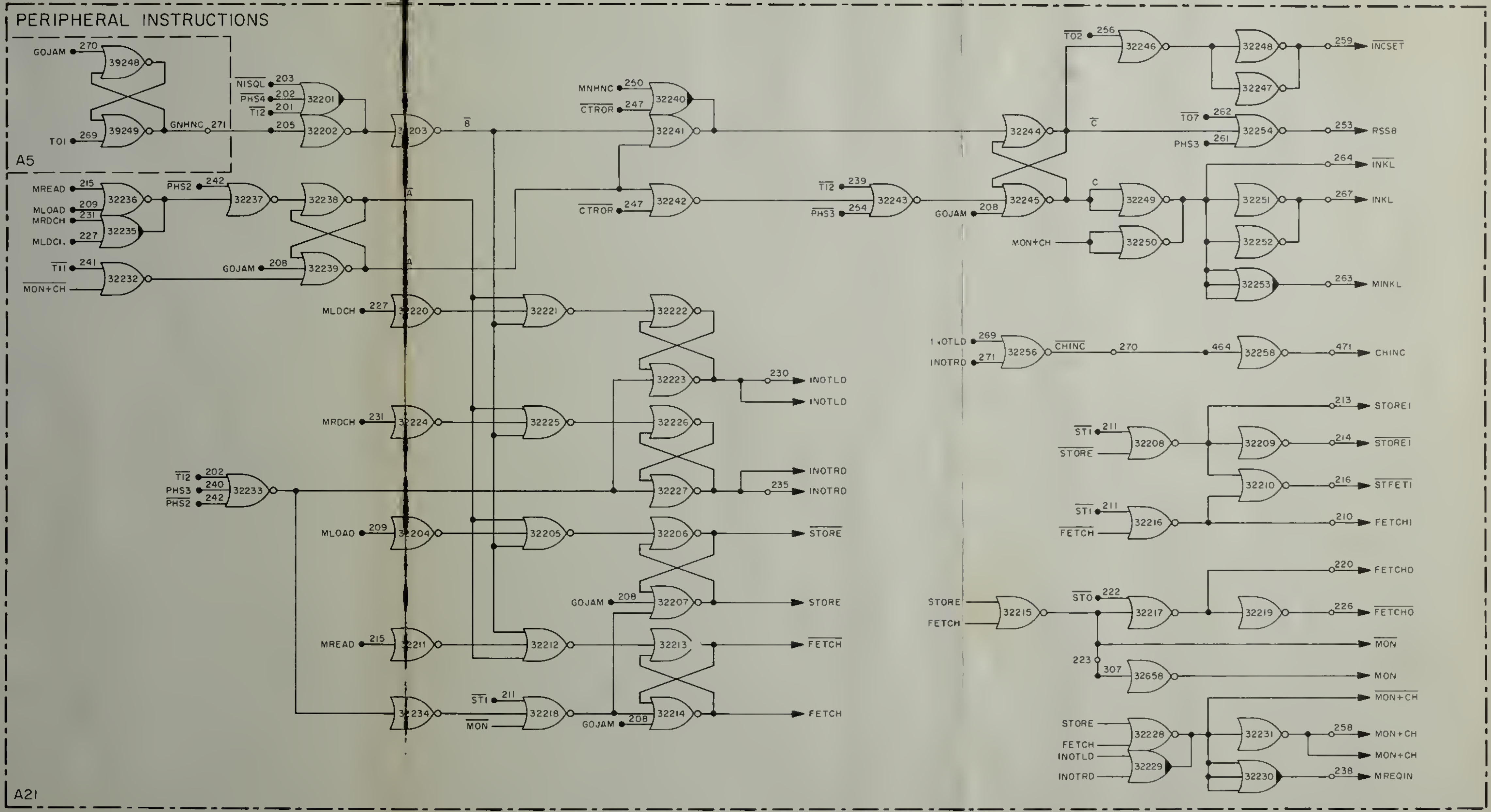

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Figure 4-133. Counter and Peripheral Instruction Control Logic (Sheet 1 of 2)

COUNTER INSTRUCTIONS	
SIGNAL	EQUATION
PINC	(C24A + C25A + C26A + C27A + C30A + C37P + C40P + C41P + C42P + C43P + C44P) INCSET + PINC $\overline{\text{T12}}$
MINC	(C37M + C40M + C41M + C42M + C43M + C44M) INCSET + MINC $\overline{\text{T12}}$
PCDU	(C32P + C33P + C34P + C35P + C36P) INCSET + PCDU $\overline{\text{T12}}$
MCDU	(C32M + C33M + C34M + C35M + C36M) INCSET + MCDU $\overline{\text{T12}}$
SHINC	(C45M + C46M + C57A + C60A) INCSET + SHINC $\overline{\text{T12}}$
SHANC	(C45P + C46P) INCSET + SHANC $\overline{\text{T12}}$
DINC	(C31A + C47A + C50A + C51A + C52A + C53A + C54A + C55A + C56) INCSET + DINC $\overline{\text{T12}}$

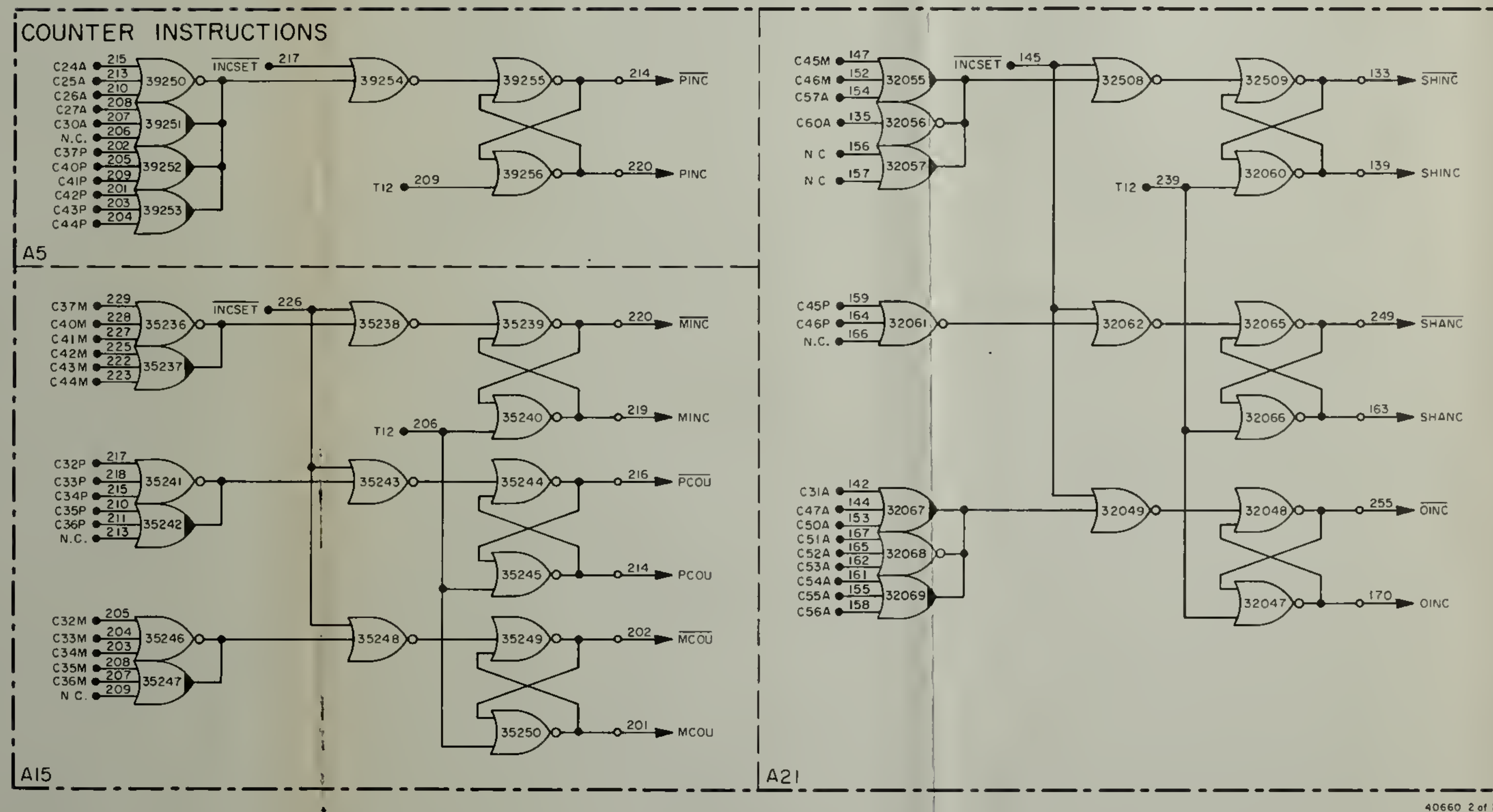

Figure 4-133. Counter and Peripheral Instruction Control Logic (Sheet 2 of 2)

signal STORE1. In addition, when signals T12, PHS2, MON, and ST1 are all present, the STORE flip-flop is reset. This condition occurs at the end of the second MCT. Signal STORE also produces signal MON+CH which resets the A flip-flop at time pulse T11. The STORE flip-flop may be reset at any time by signal GOJAM.

The FETCH flip-flop is set when signals MREAD, A, and B are present. Signal FETCH produces signals MON and MON+CH. During the first MCT of instruction FETCH, signal MON and ST0 produce instruction command FETCH0. During the second MCT, signals FETCH and ST1 produce signal FETCH1. Instruction command STFET1 is produced by either FETCH1 or STORE1. The FETCH flip-flop is reset at time pulse T12 when signals PHS2, MON, and ST1 are all present. It may also be reset by signal GOJAM. Signal MREQIN is sent to the peripheral equipment to indicate that the computer has accepted the instruction request and to control the circuits which supply signals MREAD, MLOAD, MRDCH, and MLDCH.

The priority control supplies instruction signals to the counter and peripheral instruction control. The priority control contains 29 counter cell circuits, one for each counter location in erasable memory. Each counter performs a particular function. For example, time counters T1 through T5 are incremented at regular intervals to provide elapsed time data for the program. Since these counters can only be incremented, they are controlled by instruction PINC. Other counters can be incremented or decremented by instructions PINC or MINC, respectively, or by instructions PCDU or MCDU when dealing with the CDU counters. Other counters are controlled by instructions SHINC, SHANC, and DINC.

When any counter is to be updated the associated cell in the priority control is set by an incremental pulse input. The cell then produces a counter address signal. For example, if the counter at location 0024 is to be updated, cell 24 is set and counter address signal C24A is produced. The counter address signal then performs as many as two functions. First, if the counter being updated is controlled by only one instruction such as instruction PINC, the counter address signal sets the associated instruction flip-flop in the counter and peripheral instruction control. Then, as the instruction is being executed, the counter address signal produces the corresponding octal address which is placed onto the write lines and written into register S by control pulse action.

Since certain counters are controlled by two instructions, their counter address signals cannot be used to set an instruction flip-flop in the counter and peripheral instruction control. The cells in the priority control for these counters produce one of two signals in addition to the counter address signal. The additional signals are produced by flip-flop in the cell circuit. If a counter is to be decremented, one of the two flip-flops will be set by an incremental input. If the same counter must be incremented at later time, the other flip-flop is set by a different incremental input. The signals from these flip-flops are labeled with a P or an M to indicate a plus increment or minus increment, respectively. For example, when counter 0037 is being incremented, signal C37P is produced. This signal sets the PINC flip-flop in the counter and peripheral instruction control. When the same counter is being decremented, signal C37M is produced. This signal sets the MINC flip-flop. Table 4-IX lists the counter address and instruction signals from the cells in the priority control.

Table 4-XI. Counter Cell Signals

Counter	Location	Address Signal	Instruction Signal	Instruction
T2	0024	C24A		PINC
T1	0025	C25A		PINC
T3	0026	C26A		PINC
T4	0027	C27A		PINC
T5	0030	C30A		PINC
T6	0031	C31A		DINC
CDUX	0032	C32A	C32P	PCDU
			C32M	MCDU
CDUY	0033	C33A	C33P	PCDU
			C33M	MCDU
CDUZ	0034	C34A	C34P	PCDU
			C34M	MCDU
TRN	0035	C35A	C35P	PCDU
			C35M	MCDU
SHAFT	0036	C36A	C36P	PCDU
			C36M	MCDU
PIPX	0037	C37A	C37P	PINC
			C37M	MINC
PIPY	0040	C40A	C40P	PINC
			C40M	MINC
PIPZ	0041	C41A	C40P	PINC
			C40M	MINC
BMAGX	0042	C42A	C42P	PINC
			C42M	MINC
BMAGY	0043	C43A	C43P	PINC
			C43M	MINC
BMAGZ	0044	C44A	C44P	PINC
			C44M	MINC
INLINK	0045	C45A	C45P	SHANC
			C45M	SHINC
RNRAD	0046	C46A	C46P	SHANC
			C46M	SHINC
GYRO	0047	C47A		DINC
CDUX	0050	C50A		DINC
CDUY	0051	C51A		DINC
CDUZ	0052	C52A		DINC
TRUN	0053	C53A		DINC
SHAFT	0054	C54A		DINC
THRST	0055	C55A		DINC
EMS	0056	C56A		DINC
OTLINK	0057	C57A		SHINC
ALT	0060	C60A		SHINC

The cell signals which set the various counter flip-flops are shown in figure 4-133. Only one cell signal is present at a time. Each of the counter instruction flip-flops are set at time pulse T02 as determined by signal INCSET. Signal INCSET is present only when the NISQL flip-flop is set and no peripheral instruction is being executed. The counter instruction flip-flops remain set from time pulse T02 through T12. The control pulses required at time pulse T01 of the counter instructions are produced by instruction command signal INKL.

4-5.4.10 Crosspoint Generator. The crosspoint generator receives subinstruction and instruction commands from the command generator, branch commands from the branch control, and timing pulses from the timer. It produces crosspoint or action pulses as necessary by ANDing a given command signal with the appropriate time pulse signal. The crosspoint pulses are converted into control pulses and applied to various elements of the computer for regulating data flow. Some of the crosspoint pulses are used directly as control pulses due to the function which they must perform. However, most control pulses are produced by the control pulse gates. Some crosspoint pulses are controlled by branch commands in addition to a subinstruction or instruction command. For example, subinstruction CCS0 uses branch commands during time pulses T07 and T10 as listed in table 4-VII, Machine Instructions, paragraph 4-5.2.

Subinstruction CCS0 is a decision-making subinstruction. At time pulse T01, instruction command IC12 and time pulse T01 are ANDed to produce crosspoint pulse (XP) RL10BB as shown in figure 4-134 and listed in table 4-XII. Crosspoint pulse RL10BB is also produced by commands DAS0, DAS1, IC9, DXCH0, PIRNC, or INOUT. This pulse performs several functions. First, it is used as a control pulse to place the ten (10) low order bits of register B onto the write lines. Second, it is converted into control pulse (CP) WS which enters the content of the write lines into register S.

At time pulse T02, crosspoint pulse 2B is produced and converted into control pulses RSC and WG. Signal 2B is produced involuntarily every T02 time pulse except when inhibited by subinstruction commands MP1, MP3, or DV0 or instruction commands INOUT and DV1376. Many subinstructions use control pulses RSC and WG at time pulse T02 as listed in table 4-VII. If the content of register S is an erasable memory address, control pulse WG clears register G and the decoded address signals inhibit control pulse RSC. Data from fixed or erasable memory may be transferred into it at a later time. If a central processor register is addressed, fixed and erasable memory timing is turned off, and the content of addressed register is copied into register G by control pulses RSC and WG. For subinstruction CCS0, the address in register S can be that of an erasable memory or central processor location. It can never be a fixed memory address because control pulse RL10BB does not place bits 12 and 11 of the address onto the write lines.

No crosspoint or control pulses are produced at time pulses T03 and T04 of subinstruction CCS0. However, the content of the addressed erasable memory location is entered into register G at time pulse T04.

Table 4-XII. Subinstruction CCS0

Time	BR1 and BR2	Involuntary		CCS0		IC12	
		XP	CP	XP	CP	XP	CP
1						RL10BB	WS
2		2B	RSC WG				
5				5G	RG TMZ TPZG TSGN	5J	RG WB
7	XX			7D	RZ WY12		
7	X1			7XP4	PONEX		
7	1X			PTWOX			
8		8XP10	WS	8A	RU WZ		
9						9B	RB WG
10	XX			10B	ST2 WY		
10	00			10XP9	RB		
10	X0			10XP6	CI MONEX		
10	1X			10G	RC		
11				11E	RU WA		

TOI CROSSPOINT

SIGNAL	CONTROL PULSES	EQUATION
R15	R15 WS	TOI (RSM3 + RUPT0 + RUPT1)
RB2	RB2	TOI RUPT1
1XP10	RA TMZ TSCN WB	TOI DVO
1A	C1 WY12	TOI (IC2 + IC3 + IC10)
1B	MONEX	TOI IC10
1C	RZ	TOI (IC2 + STO2)
1D	RB	TOI (TC0 + TCF0 + IC4)
RL10BB	RL10BB WS	TOI (IC12 + DAS0 + DAS1 + IC9 + DXCH0 + PRINC + INOUT)
R6	R6 WS	TOI FETCH0
1E	WS	TOI CHINC
RSCT	RSCT WS	TOI INKL $\overline{\text{MON + CH}}$

TO2 CROSSPOINT

SIGNAL	CONTROL PULSES	EQUATION
2A	WG	TO2 WRITE0
2XP3	RA WB	TO2 INOUT
2B	RSC WG	TO2 $\overline{\text{(INOUT + MP1 + MP3 + DV4 + DV1376)}}$
2XP5	RC TMZ WA	TO2 DVO $\overline{\text{BR1}}$
2C	NISQ	TO2 (IC2 + IC3 + RSM3)
OVST	DVST	TO2 DIV $\overline{\text{STO2}}$
2XP7	NISQ ZIP	TO2 MP3
2XP8	ST1 WY	TO2 FETCH0

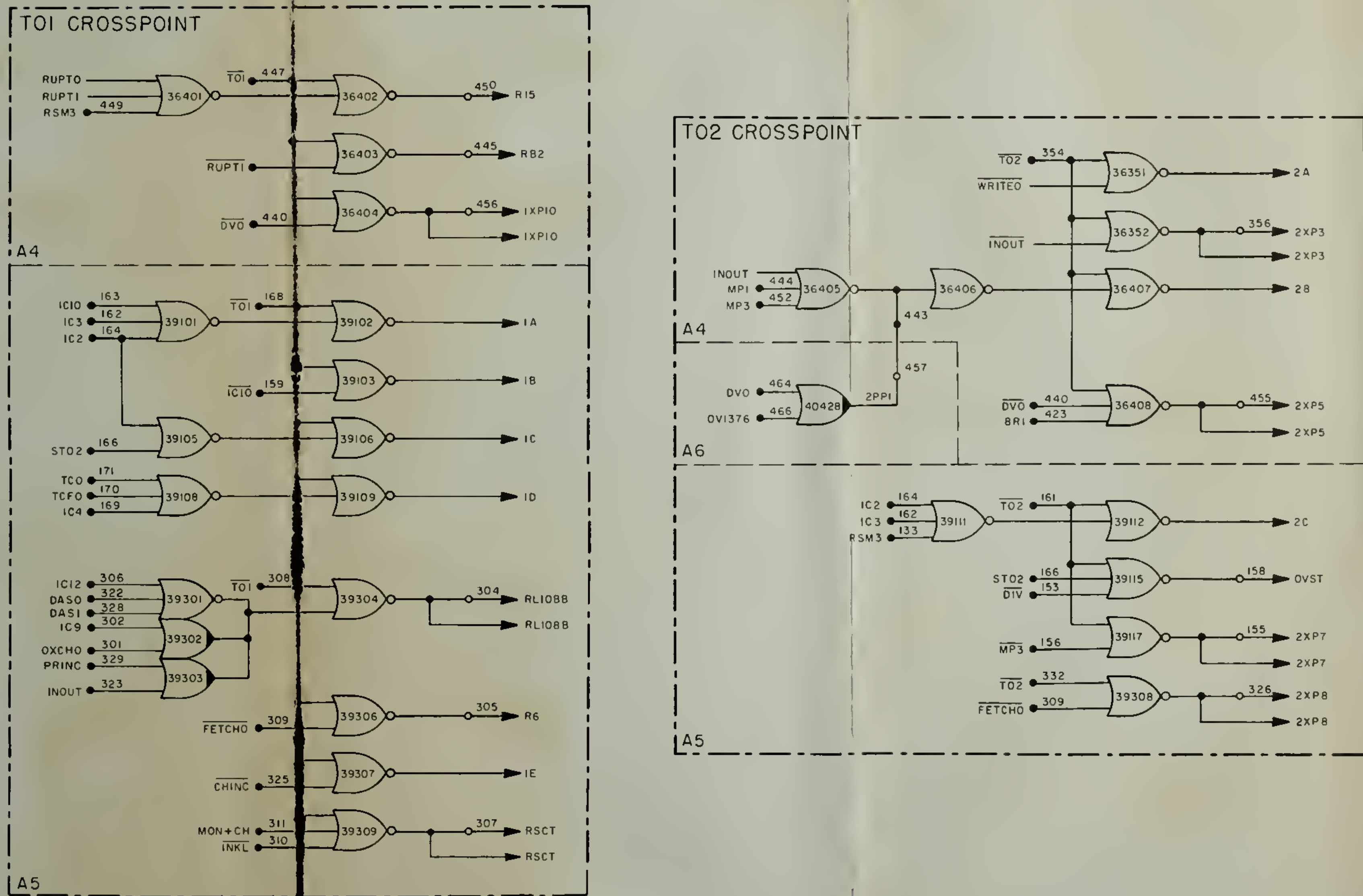

Figure 4-134. Crosspoint Generator, Logic Diagram (Sheet 1 of 10)

T03 CROSSPOINT

SIGNAL	CONTROL PULSES	EQUATION
RRPA	RRPA WZ	T03 RUPT1
3XP7	RC RCH	T03 RXORO
3A	RB	T03 (RORO + WORO)
3B	RC	T03 (RANOO + WANOO)
3C	TSGN	T03 MPO
3O	WY	T03 INOUT
3XP2	TOV	T03 TSO
3XP5	RB WZ	T03 IC2
3E	RA TMZ TSGN WG	T03 IC15
3XP6	RZ WQ	T03 TCO
3F	RA WB	T03 (OASO + TSO + MASKO + IC5 + MPO)
3G	RL WB	T03 IC8
RQ	RQ WB	T03 QXCHO

T04 CROSSPOINT

SIGNAL	CONTROL PULSES	EQUATION
4A	CI L16	T04 TSO (BR1 BR2 + $\overline{BR1}$ $\overline{BR2}$)
4B	RB WL	T04 MPO $\overline{BR1}$
4C	RC WL	T04 MPO BR1
4XP5	RZ WY12	T04 · TSO
4O	TSGN	T04 DV1 BR2
4XP11	RCH	T04 INOUT
4E	RSC WG	T04 MP3
4F	RA	T04 IC2
4G	TPZG	T04 IC15
4H	RL WA	T04 OASO
4J	RC WA	T04 MASKO
4K	RL	T04 OV1
4L	WB	T04 (OVI + INOUT + IC2)
4M	WSC	T04 MON $\overline{FETCH1}$

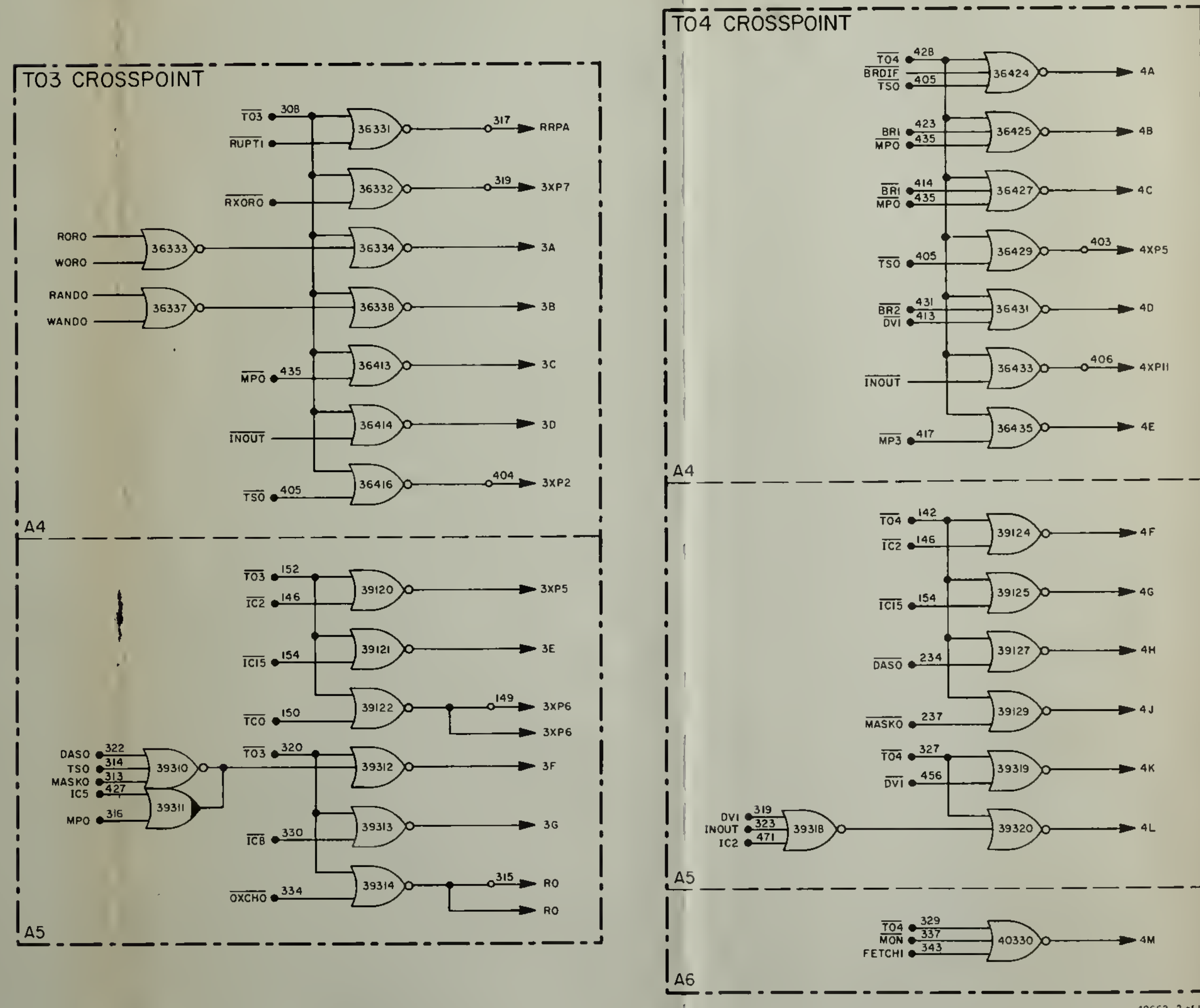

Figure 4-134. Crosspoint Generator. Logic Diagram (Sheet 2 of 10)

T05 CROSSPOINT		
SIGNAL	CONTROL PULSES	EQUATION
5XP28	RG TSGU WB	T05 DV4
5XP11	RU WA	T05 INOUT $\overline{\text{READO}}$ $\overline{\text{WRITEO}}$ $\overline{\text{RXORO}}$
5A	RB	T05 READO
5B	RA WCH	T05 WRITEO
5C	WCH	T05 WORO
5D	RA RC WG	T05 RXORO
5E	RB1	T05 TS0 $\overline{\text{BR1}}$ BR2
5F	R1C	T05 TS0 BR1 $\overline{\text{BR2}}$
B15X	B15X WY	T05 DV1
5XP4	RG WZ	T05 RSM3
5G	RG TMZ TPZG TSGN	T05 (PARTC + PRINC + CCS0)
5H	RZ	T05 IC2
5XP12	RU WL	T05 DAS0
TRSM	TRSM	T05 NDX0

T05 CROSSPOINT (cont)		
SIGNAL	CONTROL PULSES	EQUATION
5J	RG WB	T05 IC12
5K	RG A2X	T05 DAS1
5L	WY	T05 (PRINC + DAS1 + PARTC)
5XP9	RG TSGN WYD	T05 SHIFT
5M	CI	T05 SHANC
5XP13	RG WL	T05 IC8
5XP15	RG WQ	T05 OXCHO
5XP21	RCH	T05 CHINC
5N	CI RB WY12	T05 IC16
5P	CI RZ WY12	T05 MP3
5Q	RG	T05 IC5
5R	RC	T05 (DV1 BR1 + RANDO + WANDO)
Z16	Z16	T05 DV1 BR1
5XP19	RB	T05 DV1 $\overline{\text{BR1}}$ + RORO + WORO)
5S	WA	T05 TS0 ($\overline{\text{BR1}}$ BR2 + BR1 $\overline{\text{BR2}}$) + T05 (IC2 + IC5 + READO + DV4

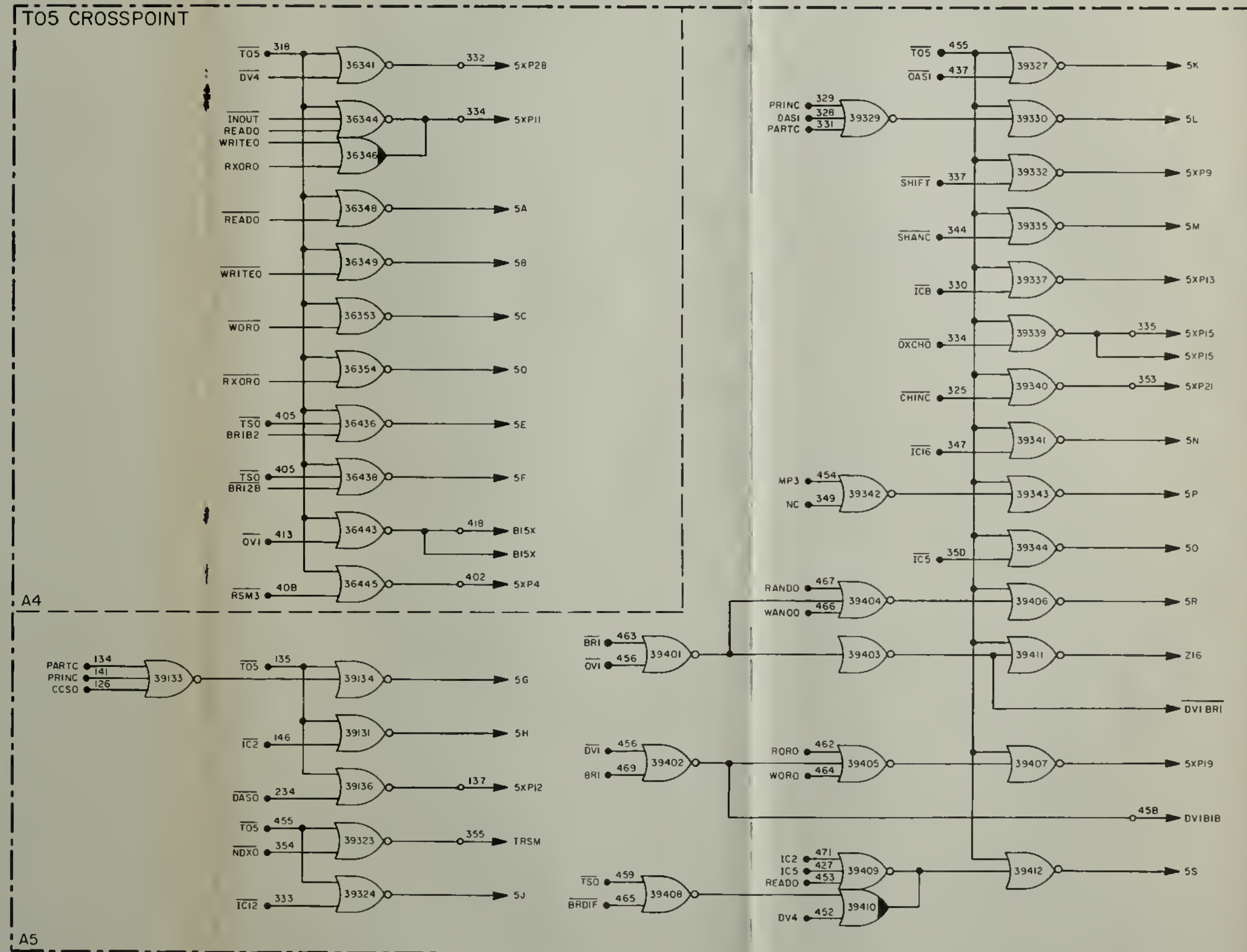

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Figure 4-134. Crosspoint Generator, Logic Diagram (Sheet 3 of 10)

T06 CROSSPOINT		
SIGNAL	CONTROL PULSES	EQUATION
6XP5	RU TOV WL	T06 DV1
TL15	TL15	T06 MP3
6A	RB WG	T06 RSM3
6B	A2X RG WY	T06 DASO
6C	A2X CI RC WY	T06 MSUO
6D	RU WZ	T06 (IC16 + MP3 + IC2 + IC3 + TS0)
6XP8	RU TOV WG WSC	T06 DAS1
6XP7	RZ TOV	T06 DV4
6XP2	RA WB	T06 $\overline{\text{RXORO}}$ INOUT
6XP10	PONEX	T06 (AUGO $\overline{\text{BR1}}$ + DIMO BR1 $\overline{\text{BR2}}$ + DINC BR1 $\overline{\text{BR2}}$ + INCRO + PINC)
6E	MONEX	T06 (MINC + MCDU + AUGO BR1 + DIMO $\overline{\text{BR1}}$ $\overline{\text{BR2}}$ + DINC $\overline{\text{BR1}}$ $\overline{\text{BR2}}$)
6XP12	CI	T06 (PCDU + MCDU)

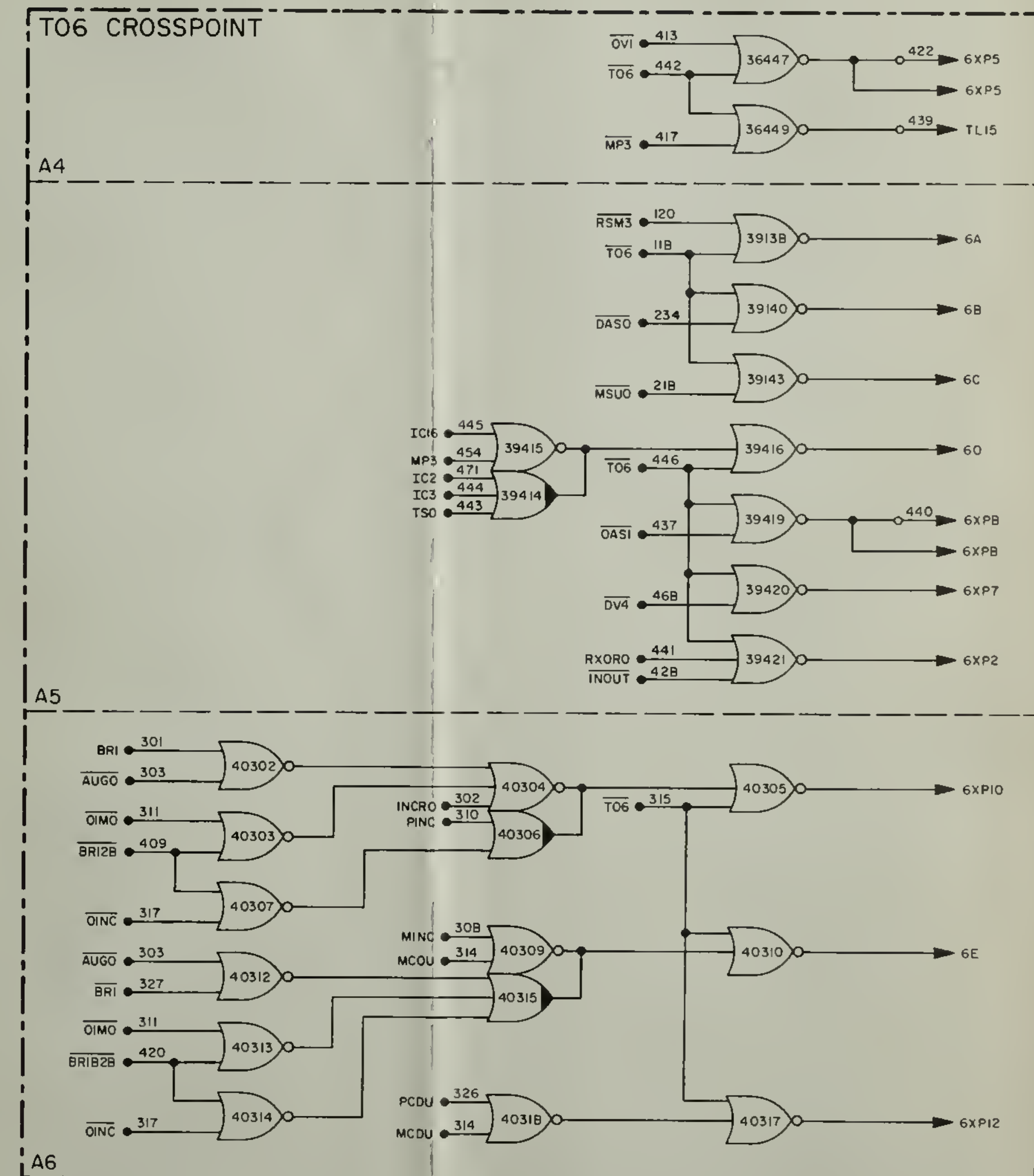


Figure 4-134. Crosspoint Generator, Logic Diagram (Sheet 4 of 10)

T07 CROSSPOINT		
SIGNAL	CONTROL PULSES	EQUATION
TSGN2	TSGN2	T07 MPO
7A	RSC TSGN	T07 OVI
7XP19	A2X RB WY	T07 MP3 BRI
7B	RB	T07 OASO
7XP9	RUS TSGN	T07 MSUO
7C	A2X RG WY	T07 IC2
7XP4	PONEX	T07 CCSO BR2
PTWOX	PTWOX	T07 CCSO BRI
7O	RZ WY12	T07 CCSO
7E	RG	T07 STFETI
7F	RG WB	T07 (IC13 + IC14 + OVI)
7G	WA	T07 (OASO + OASI + MSUO)
7XP7	RC WA	T07 OV4 (BRI + BR2) + T07 (RANOO + WANOO)
7XP14	WCH	T07 (INOTLO + WANOO)
7XP10	RBI	T07 OASI ($\overline{\text{BRI}}$ + BR2)
7XP11	RIC	T07 OASI (BRI + $\overline{\text{BR2}}$)
7XP15	RUS	T07 (PCOU + MCOU + SHIFT)
7H	RU	T07 (PRINC + PINC + MINC + OINC)
WOVR	WG WOVR WSC	T07 (MON + CH) (PRINC + INKL)
7J	RB WC WSC	T07 (IC9 + OXCHO)

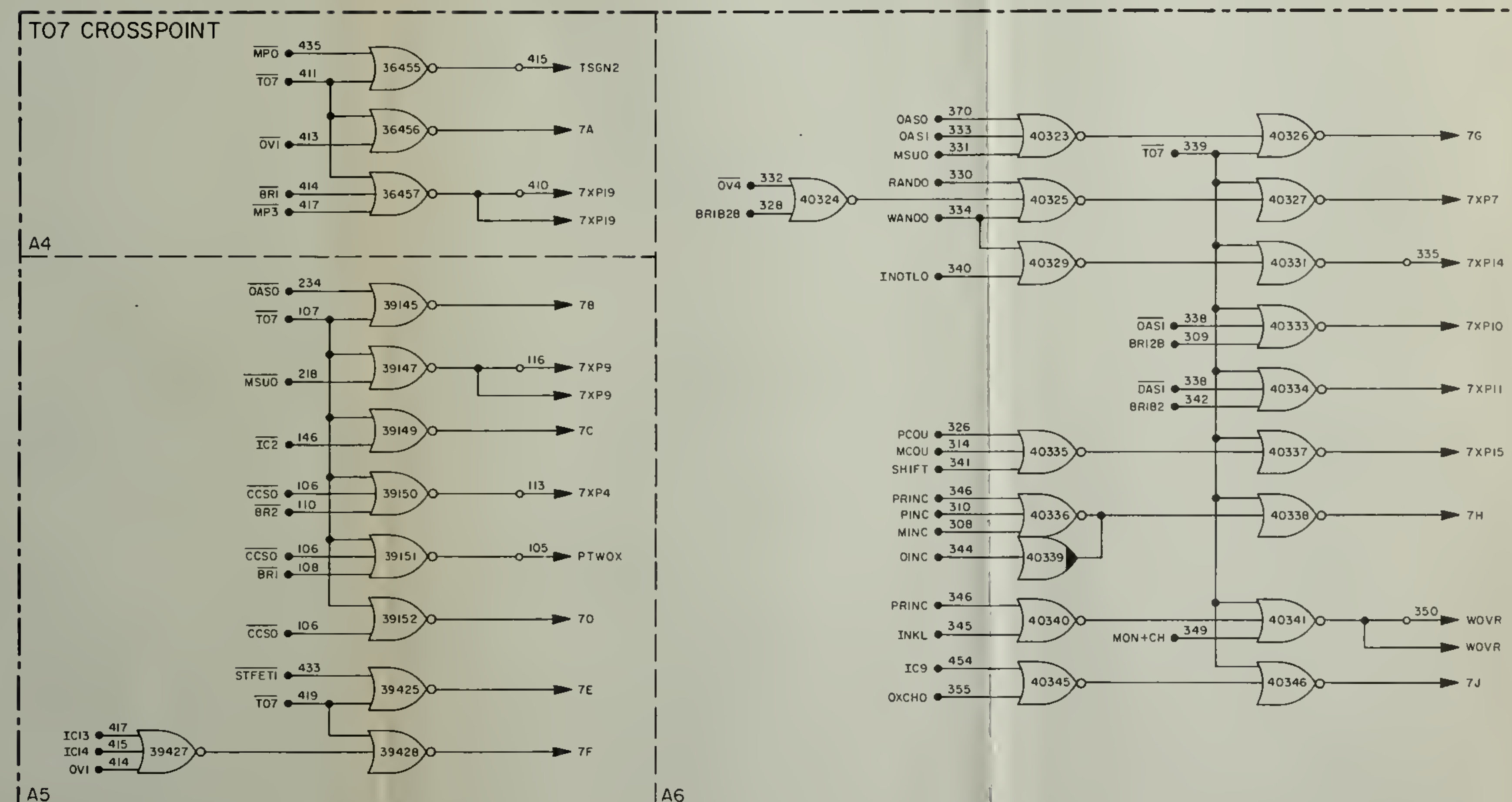


Figure 4-134. Crosspoint Generator, Logic Diagram (Sheet 5 of 10)

T08 CROSSPOINT		
SIGNAL	CONTROL PULSES	EQUATION
8A	RU WZ	T08 CCS0
3B	RB	T08 INKL $\overline{\text{FETCH0}}$
RAD	RAD WB	T08 (IC3 + RSM3 + MP3 + IC16)
8XP15	NISQ	T08 IC16
8XP3	RZ	T08 (MP0 + IC1)
8C	RU	T08 (IC2 + IC4 + DXCH0)
8D	WB	T08 (GOJ1 + DAS0 + DXCH0)
RSTRT	RSTRT	T08 GOJ1
8XP12	RL	T08 DAS0
8E	ST2 WZ	T08 TCSAJ3
U2BBK	U2BBK	T08 $\overline{\text{MONWBK}}$ STFET1
RSTSTG	RSTSTG TSGN	T08 DV4
8XP4	RZ ST2	T08 (RUPT1 + DAS1 + MSU0 + IC17 + MASK0 + IC11 + IC6 + IC7 + IC9 + INOUT + DV4 + PRINC)
8XP10	WS	T08 $\overline{\text{RUPT0}}$ $\overline{\text{DAS0}}$ $\overline{\text{MP1}}$ $\overline{\text{DV1376}}$
8XP5	RA WY	T08 DV1
8XP6	PONEX	T08 DV1 $\overline{\text{BR2}}$

T09 CROSSPOINT		
SIGNAL	CONTROL PULSES	EQUATION
9XP1	RG WG	T09 RUPT0
9A	RC WG	T09 RXOR0
9B	RB WG	T09 (RUPT1 + IC13 + IC12)
9C	WG	T09 STORE1
9D	RB WY	T09 MP0 $\overline{\text{BR1}}$
9E	RC WY	T09 MP0 BR1
9F	CI	T09 MP0 ($\overline{\text{BR1}}$ BR2 + BR1 $\overline{\text{BR2}}$)
9G	RA	T09 MP3
KRPT	KRPT	T09 RUPT1
9H	RB WA	T09 (IC2 + DV1 $\overline{\text{BR1}}$)
9XP5	RU TOV WG WSC	T09 DAS0
9J	RA RC WY	T09 MASK0
9K	RC WA Z15	T09 DV4
9L	RU WB WL	T09 DV4
9M	RC TMZ	T09 DAS1

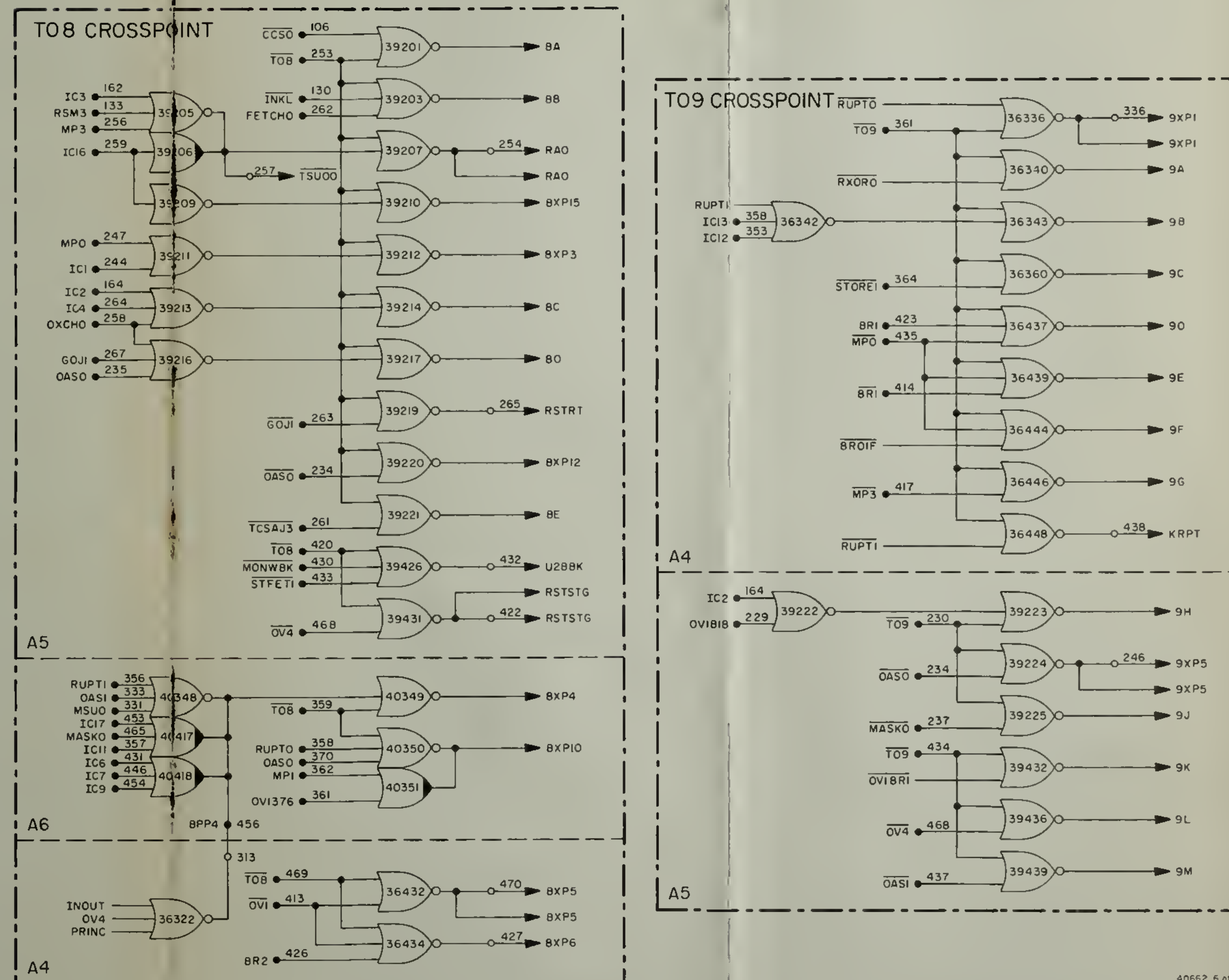


Figure 4-134. Crosspoint Generator, Logic Diagram (Sheet 6 of 10)

TIO CROSSPOINT		
SIGNAL	CONTROL PULSES	EQUATION
MPOTIO	ST1 TSGN	T10 MPO
10A	RL	T10 MP3
10B	ST2 WY	T10 · CCSO
10XP6	CI MONEX	T10 CCSO $\overline{\text{BR2}}$
10XPI	ST1	T10 · (IC1 + IC10 + RUPTO)
10C	RA WY	T10 (OASO + MSUO BR1)
10XP7	MONEX	T10 (MSUO BR1 + OASO BR1 $\overline{\text{BR2}}$)
10XP8	PONEX	T10 · OASO BR1 BR2
10D	RU WB	T10 · (IC14 + IC2 + OV1)
10XP10	A2X WY	T10 IC11
10E	WL	T10 (IC4 + OV4 $\overline{\text{BR1}}$ + OASI $\overline{\text{AOSO}}$ $\overline{\text{BR2}}$)
EXT	EXT	T10 NOXX1
10XP9	RB	T10 (IC6 + OCAO + AOO + CCSO $\overline{\text{BR1}}$ $\overline{\text{BR2}}$)
10F	WA	T10 (IC6 + IC7)
10G	RC	T10 (IC7 + OCSO + SUO + CCSO BR1 $\overline{\text{BR2}}$ + OV4 $\overline{\text{BR1}}$)
10XP15	ST1 ST2	T10 MP1

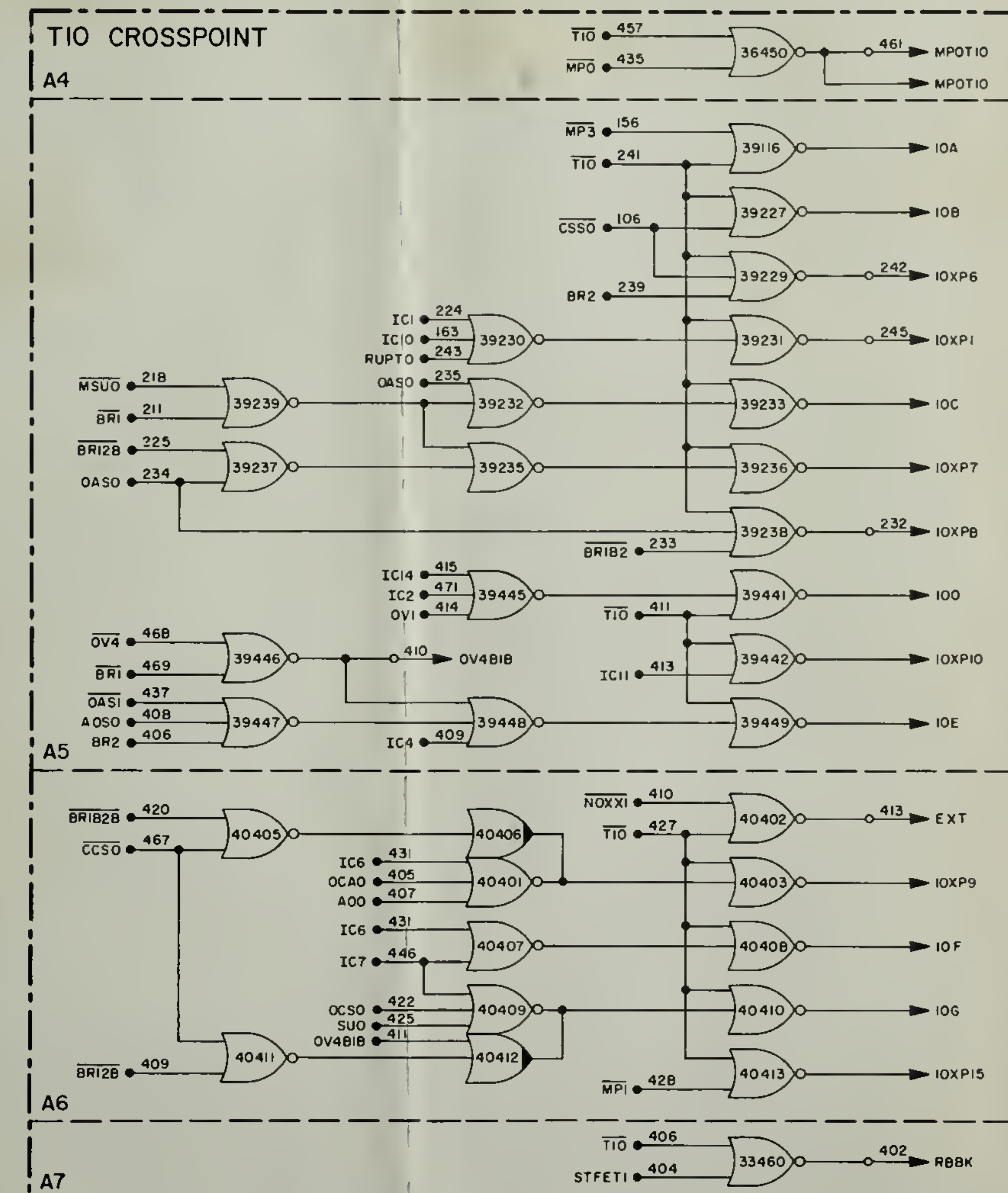


Figure 4-134. Crosspoint Generator, Logic Diagram (Sheet 7 of 10)

T11 CROSSPOINT		
SIGNAL	CONTROL PULSES	EQUATION
11A	R1C RBI	T11 MP0 BR1
11XP2	RUS	T11 MSU0
11B	RC	T11 MASK0
11C	WA	T11 (MSU0 + IC14)
11XP6	RL WYO	T11 DV1
11D	RC RG	T11 RXOR0
11E	RY WA	T11 (CCS0 + MP3 BR1 + DAS0 + ADS0 + IC11 + DAS1 BR2)

T12 CROSSPOINT		
SIGNAL	CONTROL PULSES	EQUATION
12A	RU	T12 T12USE OV1

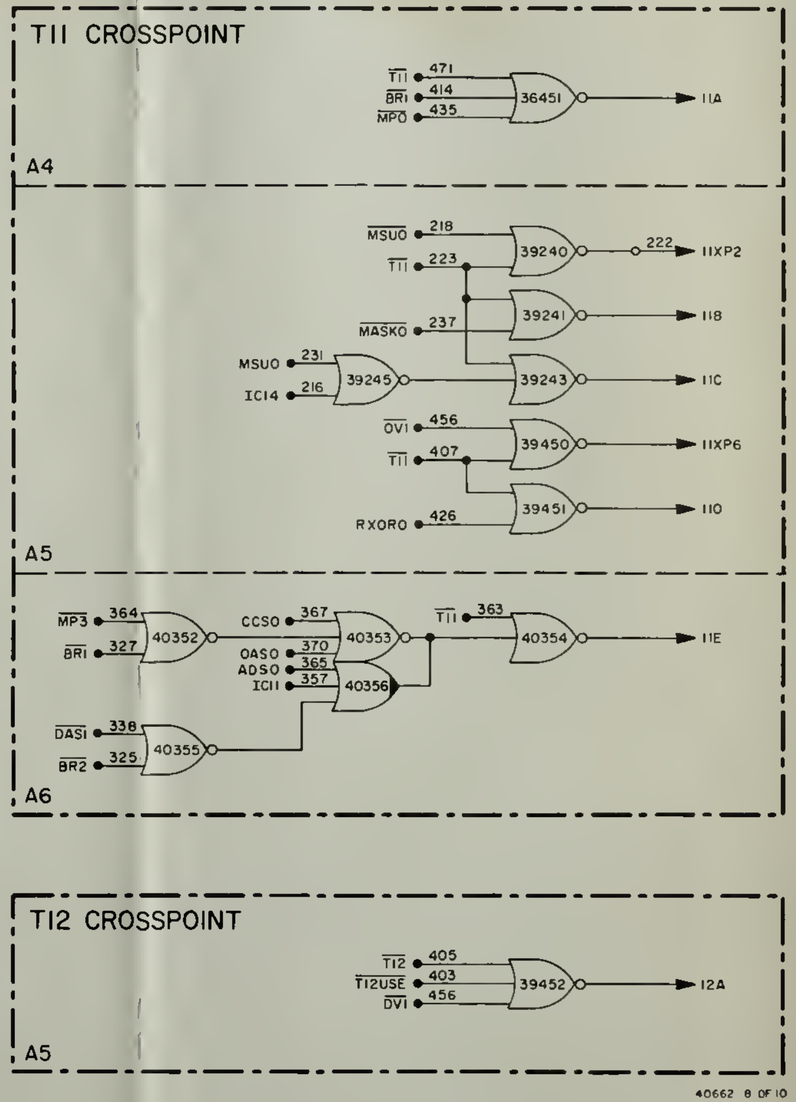
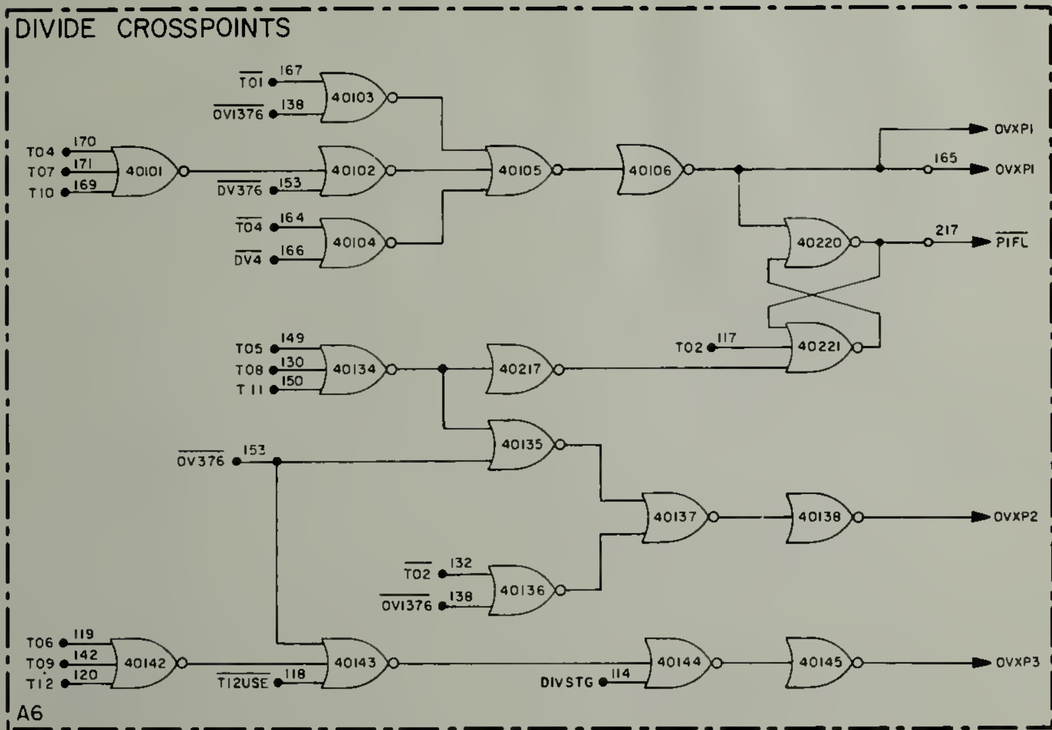


Figure 4-134. Crosspoint Generator, Logic Diagram (Sheet 8 of 10)



DIVIDE CROSSPOINTS		
SIGNAL	CONTROL PULSES	EQUATION
DVXP1	A2X L2GD RB WYD	DV1376 T01 + DV376 (T04 + T07 + T10) + DV4 T04
PIFL	PIFL	DVXP1 + $\overline{\text{(T02 + T05 + T08 + T11)}}$ PIFL
DVXP2	RG TSGU WL	DV1376 T02 + DV376 (T05 + T08 + T11)
DVXP3	RU WB	DV376 (T06 + T09 + T12) T12 USE + DIVSTG

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Figure 4-134. Crosspoint Generator, Logic Diagram (Sheet 9 of 10)

MULTIPLY CROSSPOINTS		
SIGNAL	CONTROL PULSES	EQUATION
ZIP	A2X L2GO	$2XP7 + MP1\ (T01 + T03 + T05 + T07 + T09 + T11)$
MPXP1	WY	$ZIP\ (\overline{\overline{L15}\ L02\ \overline{L01}})\ (\overline{L15\ \overline{L02}\ L01})$
MPXP2	WYO	$ZIP\ (\overline{L15}\ L02\ \overline{L01} + L15\ \overline{L02}\ L01)$
MCRO	MCRO	$ZIP\ L02\ (\overline{\overline{L15}\ L02\ \overline{L01}})$
ZIPCI	RC CI	$ZIP\ L02\ (\overline{\overline{L15}\ L02\ \overline{L01}})\ (\overline{L15\ L02\ L01})$
MPXP3	RB	$ZIP\ (\overline{L02} + \overline{L15}\ L02\ \overline{L01})\ (\overline{\overline{L15}\ \overline{L02}\ \overline{L01}})$
ZAP	G2LS RU WALS	$MP1\ (T02 + T04 + T06 + T08 + T10) + MP3\ (T01 + T03)$

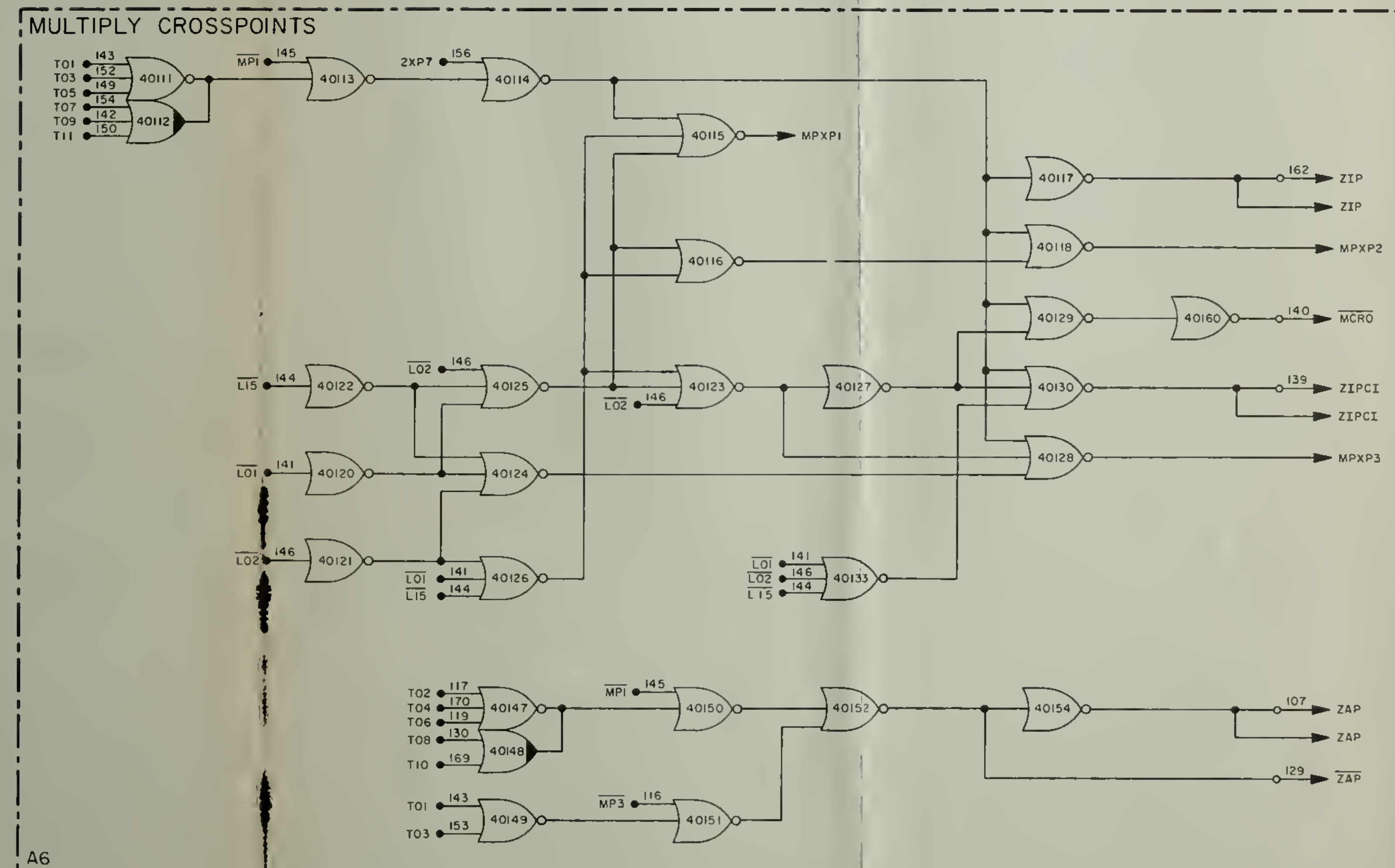

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Figure 4-134. Crosspoint Generator, Logic Diagram (Sheet 10 of 10)

At time pulse T05, crosspoint pulses 5G and 5J are produced from commands CCS0 and IC12, respectively. Crosspoint pulse 5G may also be produced from command PARTC or PINC. Crosspoint pulse 5G produces control pulses RG, TMZ, TPZG, and TSGN. Control pulse RG places the content of register G onto the write lines. The branch flip-flops are set to the 00 state if register G and the write lines contain a positive quantity. Control pulse TSGN resets the branch 1 flip-flop and control pulses TMZ and TPZG reset the branch 2 flip-flop. Branch state 01 is established if register G contains a plus zero. Control pulse TSGN resets the branch 1 flip-flop and control pulse TPZG, in conjunction with the decoded output of register G, sets the branch 2 flip-flop. Branch state 10 is established if the write lines contain a negative quantity other than minus zero. Control pulse TSGN, in conjunction with signal WL16, sets the branch 1 flip-flop and control pulses TPZG and TMZ reset the branch 2 flip-flop. Finally, state 11 is established when the write lines contain minus zero. The branch 1 flip-flop is set by control pulse TSGN and signal WL16. The branch 2 flip-flop is set by signals WL16 through WL01 and control pulse TMZ. The output of the branch flip-flops are decoded into various branch command signals that are used for producing crosspoint pulses.

Crosspoint pulse 5J is converted into control pulses RG and WB. Control pulse RG is also produced from crosspoint pulse 5G, thus making one RG control pulse redundant. Control pulse RG places the content of register G onto the write lines. Control pulse WB transfers the write line information into register B. Crosspoint pulse 5J can only be produced by time pulse signal T05 and instruction command signal IC12. No crosspoint pulses are produced at time pulse T06 of subinstruction CCS0.

At time pulse T07, the state of the branch flip-flops determines what crosspoint pulses are produced. The control pulses at time pulse T07 will add plus zero, one, two, or three to the address c(Z) contained in register Z if the branch flip-flops are in state 00, 01, 10, or 11, respectively. Crosspoint pulse 7D is produced by signals T07 and CCS0 and is not dependent on the state of the branch flip-flops. Signal 7D is converted into control pulses RZ and WY12 which copy the twelve (12) low order bits of register Z into the adder register Y. Control pulse WY12 also clears adder register X and the carry flip-flop. If the branch flip-flops are in the 00 state, no further action occurs at time pulse T07 and the adder gates U contain c(Z) + 0 = c(Z). If the branch 2 flip-flop is set as it is for states 01 and 11, crosspoint pulse 7XP4 is produced. Signal 7XP4 is produced by time pulse T07, subinstruction command CCS0, and branch signal BR2. Crosspoint pulse 7XP4 is then converted into control pulse PONEX which sets bit 1 of adder register X. If the branch flip-flops are in the 01 state, no further action occurs at time pulse T07. As a result, the adder gates U contain c(Z) + 1. If the branch flip-flops are in the 11 state, crosspoint pulse PTWOX is produced by signals T07, CCS0, and BR1. Signal PTWOX, which is used as the control pulse, sets bit 2 of register X. Since register X now contains octal three from the action of control pulses PONEX and PTWOX, the adder output gates contain c(Z) + 3. Had the branch flip-flops been set to state 10, only control pulse PTWOX would be produced and the output gates U would contain c(Z) + 2.

At time pulse T08, crosspoint pulse 8XP10 is produced and converted to control pulse WS. Signal 8XP10 is produced involuntarily every T08 time pulse except when inhibited by subinstruction commands RUPT0, DAS0, or MP1 or instruction command DV1376. Control pulse WS is used for copying an address into register S. The address usually comes from register Z; however, it may also come from the priority control, peripheral equipment, register B or adder gates. Signals T08 and CCS0 also produce crosspoint pulse 8A which is converted to control pulses RU and WZ. Control pulses RU, WZ, and WS enter the content of the adder gates U into registers Z and S. At time pulse T09, crosspoint pulse 9B is produced from signals T09 and IC12 and converted into control pulses RB and WB. Crosspoint pulse 9B may also be produced by signal RUPT1 or IC13. Control pulses RB and WB copy the content of register B into register G. This is the quantity that was originally taken out of erasable memory at time pulse T04 and entered into register G. The content of register G is returned to its erasable memory location at time pulse T10. This action does not destroy the same data contained in register B.

Also at time pulse T10, control pulses WY and ST2 are produced from crosspoint pulse 10B. Control pulse ST2 sets the primary level flip-flops of the stage counter to 010 in preparation for subinstruction STD2. Control pulse WY clears register X and enters the content of the write lines into register Y. If the branch flip-flops are set to state 01 or 11, no additional crosspoint and control pulses are produced. As a result, the adder gates U contain plus zero. If the branch 2 flip-flop is reset, as it is for states 00 and 10, crosspoint pulse 10XP6 is produced and converted to control pulses C1 and MONEX. Control pulse CI sets the carry flip-flop and control pulse MONEX sets register X to minus one or octal 177776. Crosspoint pulse 10XP6 is produced by signals T10 and CCS0, when signal BR2 is not present. If the quantity c(E) taken from erasable memory is positive, the branch flip-flops will be in the 00 state. Crosspoint pulse 10XP9 will produce control pulse RB which in turn will copy the positive quantity in register B onto the write lines. Control pulse WY will then enter c(E) into register Y. The quantity c(E) in register Y, minus one in register X, and a carry bit results in c(E) -1 at the output gates U. If the original quantity in erasable memory was negative c(E), the branch flip-flops will be in state 10, and crosspoint pulse 10G will produce control pulse RC. Control pulse RC converts the negative quantity c(E) in register B into the equivalent positive quantity c(E) by gating the complement output of register B onto the write lines. As a result, the same net results are obtained as with a positive quantity, namely c(E) -1 at output gates U. Crosspoint pulse 10G is also produced by commands IC7, DCS0, SU0, and a particular branch condition during DV4.

The last action of subinstruction CCS0 occurs at time pulse T11 during which crosspoint pulse 11E is produced and converted into control pulses RU and WA. These control pulses cause the content of adder gates U to be copied into register A. Crosspoint pulse 11E is also produced from signals DAS0, ADS0, IC11, and particular branch conditions of MP3 and DAS1. Subinstruction CCS0 is followed by subinstruction STD2.

Special attention is given to the divide instruction because the crosspoint circuit, which produces pulses DVXP1 through DVXP3 and PIFL, differs from the T01 through T12 crosspoint circuits (figure 4-134). The crosspoint and control pulses for subinstructions DV0, DV1, DV3, DV7, DV6, and DV4 are listed in tables 4-XIII through 4-XVII.

Table 4-XIII. Subinstruction DV0

Time	BR1 and BR2	Involuntary		DV0		DIV	
		XP	CP	XP	CP	XP	CP
1				1XP10	RA TMZ TSGN WB		
2	XX	△1				DVST	
2	0X			2XP5	RC TMZ WA		
3	△2	DIVSTG (DVXP3)	RU WB				

△1 Crosspoint pulse 2B is inhibited by command DV0.

△2 Crosspoint pulse DIVSTG is involuntary during the DV instruction. Crosspoint pulse DIVSTG also produces signal DVXP3 which is converted into control pulses RU and WB.

Table 4-XIV. Subinstruction DV1, Part 1

Time	BR1 and BR2	Involuntary		DV1	
		XP	CP	XP	CP
4	XX			4K 4L	RL WB
4	X1			4D	TSGN
5	XX			B15X	WY
5	0X			5XP19	RB
5	1X			5R Z16	RC
6				6XP5	RU TOV WL
7				7A 7F	RSC TSGN RG WB
8	XX			8XP5	RA WY
8	X0	⚠1		8XP6	PONEX
9	0X			9H	RB WA
9	1X			9K	RC WA Z15
10				10D	RU WB
11				11XP6	RL WYD
12				12A	RU WL

⚠1 Crosspoint pulse 8XP10 is inhibited by command DV1.

Table 4-XV. Subinstructions DV3, DV7, and DV6, Part 1

Time	BR1 and BR2	Involuntary		DV376	
		XP	CP	XP	CP
4				DVXP1	A2X L2GD RB WYD
				PIFL	
5	XX			DVXP2	RG TSGU WL
5	0X				CLXC
5	1X				RB1 F
6				DVXP3	RU WB
7				DVXP1	A2X L2GD RB WYD
				PIFL	
8	XX	$\triangle 1$		DVXP2	RG TSGU WL

Time	BR1 and BR2	DV376	
		XP	CP
8	0X		CLXC
8	1X		RB1 F
9		DVXP3	RU WB
10		DVXP1	A2X L2GD RB WYD
		PIFL	
11	XX	DVXP2	RG TSGU WL
11	0X		CLXC
11	1X		RB1 F
12		DVXP3	RU WB

$\triangle 1$ Crosspoint pulse 8XP10 is inhibited by command DV1376.

Table 4-XVI. Subinstructions DV1, DV3, DV7, and DV6, Part 2

Time	BR1 and BR2	Involuntary		DV1376		DIV	
		XP	CP	XP	CP	XP	CP
1				DVXP1 PIFL	A2X L2GD RB WYD		
2	XX	△1		DVXP2	RG WL TSGU	DVST	
2	0X				CLXC		
2	1X				RB1F		
3	△2	DIVSTG (DVXP3)	RU WB				

△1 Crosspoint pulse 8XP10 is inhibited by command DV1376.

△2 Crosspoint pulse DIVSTG produces signal DVXP3 which is converted into control pulses RU and WB.

Table 4-XVII. Subinstruction DV4

Time	BR1 and BR2	Involuntary		DV4	
		XP	CP	XP	CP
4				DVXP1	A2X L2GD RB WYD
				PIFL	
5	XX			5XP28	RG TSGU WB
				5S	WA
5	0X				CLXC
5	1X				RB1F
6				6XP7	RZ TOV
7	X1			7XP7	RC WA
7	1X			7XP7	RC WA
8		8XP10	WS	RSTSTG 8XP4	TSGN RZ ST2
9				9L	RU WB WL
10	0X			10E 10G	WL RC

The crosspoint and control pulses for subinstruction DV0 and part 1 of subinstruction DV1 (tables 4-XIII and 4-XIV) are produced in the conventional manner by the T01 through T12 crosspoint circuits. The crosspoint pulses listed in tables 4-XV and 4-XVI and some of those listed in table 4-XVII are produced by the divide crosspoint circuit. This circuit is controlled by instruction commands DV1376 and DV376; subinstruction command DV4; signals DIVSTG and T12USE; and all time pulses except T03. Instruction command DV1376 is used to produce crosspoint pulse DVXP1 at time pulse T01. Crosspoint pulse DVXP1 is also produced at time pulse T04, T07, and T10 by instruction command DV376 and at time pulse T04 by subinstruction command DV4. Crosspoint pulse DVXP1 is converted into control pulses A2X, L2GD, RB, and WYD, by the control pulse gates. Control pulses CLXC and RB1F are discussed in detail in the branch control circuit description.

Signal DVXP1 is also applied to the set side of the PIFL flip-flop. Signals DVXP1 and PIFL occur simultaneously since the reset side of the PIFL flip-flop is pulsed at time pulses T02, T05, T08, and T11.

Crosspoint pulse DVXP2 is produced at time pulse T02 by instruction command DV1376 and at time pulses T05, T08, and T11 by instruction command DV376. This signal is converted into control pulses RG, TSGU, and WL.

Control pulse DIVSTG occurs at time pulse T03 of the divide subinstructions and produces crosspoint pulse DVXP3. Signal DVXP3 is also produced at time pulses T06, T09, and T12 when signals DV376 and T12USE are present. Signal T12USE is a flip-flop signal produced by the stage counter and decoder circuit. Crosspoint pulse DVXP3 is converted into control pulses RU and WB.

The multiply instruction also requires special consideration because the multiply crosspoint circuit differs from the conventional T01 through T12 crosspoint circuits. The multiply crosspoint circuit produces signals ZIP, ZAP, MPXP1, MPXP2, MPXP3, MCRO, and ZIPCI, as shown in figure 4-134 and listed in tables 4-XVIII through 4-XXI. Crosspoint pulse ZIP is converted into control pulses A2X and L2GD and is produced at time pulses T01, T03, T05, T07, T09, and T11 of subinstruction MP1. It is also produced by crosspoint pulse 2XP7 which occurs at time pulse T02 during subinstruction MP3.

Table 4-XVIII. Subinstruction MP0

Time	BR1 and BR2	Involuntary		MP0		IC14	
		XP	CP	XP	CP	XP	CP
2		2B	RSC WG				
3				3C 3F	TSGN RA WB		
4	0X			4B	RB WL		
4	1X			4C	RC WL		
7				TSGN2		7F	RG WB
8		8XP10	WS	8XP3	RZ		
9	0X			9D	RB WY		
9	1X			9E	RC WY		
9	01			9F	CI		
9	10			9F	CI		
10		△1		MP0T10 10A	ST1 TSGN RL	10D	RU WB
11	XX					11C	WA
11	1X			11A	R1C RB1		

△1 Control pulse NEACON is produced in the adder at time period T10 and inhibits end around carry.

Table 4-XIX. Subinstruction MP1

Time	BR1 and BR2	Involuntary		MP1	
		XP	CP	XP	CP
1			△2	ZIP	A2X L2GD
2		△1		ZAP	G2LS RU WALS
3				ZIP	A2X L2GD
4				ZAP	G2LS RU WALS
5				ZIP	A2X L2GD
6				ZAP	G2LS RU WALS
7				ZIP	A2X L2GD
8				ZAP	G2LS RU WALS
9				ZIP	A2X L2GD
10				ZAP	G2LS RU WALS
				10XP15	ST1 ST2
11				ZIP	A2X L2GD

△1 Crosspoint pulses 2B and 8XP10 are inhibited by command MP1.

△2 See table 4-XXI for additional crosspoint pulses produced by ZIP.

Table 4-XX. Subinstruction MP3

Time	BR1 and BR2	Involuntary		MP3	
		XP	CP	XP	CP
1				ZAP	G2LS RU WALS
2		△1	△2	ZIP	A2X L2GD
3				ZAP	G2LS RU WALS
4				4E	RSC WG
5				5P	RZ WY12 CI
6		△3		TL15 6D	 RU WZ
7	1X			7XP19	A2X RB WY
8		8XP10	WS	RAD	WB
9				9G	RA
10				10A	RL
11	1X			11E	RU WA

△1 Crosspoint pulse 2B is inhibited by command MP3.

△2 See table 4-XXI for additional crosspoint pulses produced by ZIP.

△3 Control pulse NEACOF is produced in the adder at time period T06 and permits end around carry.

Table 4-XXI. Crosspoint Pulse ZIP

c(L)	ZIP	
15, 2, 1	XP	CP
000	MPXP1	WY
001	MPXP1 MPXP3	WY RB
010	MPXP2 MPXP3	WYD RB
011	MPXP1 ZIPCI MCR0	WY RC CI
100	MPXP1 MPXP3	WY RB
101	MPXP2 MPXP3	WYD RB
110	MPXP1 ZIPCI MCR0	WY RC CI
111	MPXP1 MCR0	WY

Crosspoint pulses MPXP1 through MPXP3, MCRO, and ZIPCI are dependent on the state of bits 15, 2, and 1 of register L and are produced in conjunction with crosspoint pulse ZIP. Table 4-XXI lists the crosspoint and control pulses produced by signal ZIP for all possible states of these bits. Crosspoint pulse MPXP1 is produced and converted into control pulse WY for all states except 010 and 101. During states 010 and 101, crosspoint pulse MPXP2 is produced instead of MPXP1 and converted into control pulse WYD. Control pulse RB is produced from crosspoint pulse MPXP3 during states 001, 010, 100, and 101 whereas control pulses RC and CI are produced from ZIPCI during states 011 and 110. In addition, crosspoint pulse MCRO is produced during states 011, 110, and 111 and used directly as a control pulse.

Crosspoint pulse ZAP is produced and converted into control pulses G2LS, RU, and WALS at time pulses T02, T04, T06, T08, and T10 of subinstruction MP1. It is also produced at time pulses T01 and T03, during subinstruction MP3.

During the multiply instruction, the adder is switched to perform arithmetic in the two's complement system. Switching is accomplished by signal NEACON which occurs at time pulse T10 of subinstruction MP0. Signal NEACON sets a flip-flop (part of the adder) which inhibits end around carry until it is reset by signal NEACOF at time pulse T06 of subinstruction MP3.

Tables 4-XXII through 4-LXXIV list the crosspoint and control pulses produced for the remaining subinstructions.

4-5.4.11 Control Pulse Gates. The control pulse gates (figure 4-135) convert crosspoint pulses into control pulses. For example, control pulse NISQ is produced by crosspoint pulse 2C, 2XP7, or 8XP15. A single crosspoint pulse may produce several control pulses. For example, crosspoint pulse 2XP5 produces control pulses RC, TMZ, and WA. Two control pulses, CLXC and RB1F, produced from control pulse TSGU, signal PHS4, and a branch signal, occur during the divide instruction. Only one is produced at a time. Control pulse CLXC is produced when the branch flip-flops are in the 0X state and control pulse RB1F is produced during the 1X state. Control pulse TSGU is produced by crosspoint pulse 5XP28 or DVXP2. Table 4-LXXV lists all of the control pulses produced by the control pulse gates and other circuits.

Table 4-XXII. Subinstruction STD2

Time	BR1 and BR2	Involuntary		STD2		IC3	
		XP	CP	XP	CP	XP	CP
1				1C	RZ	1A	WY12 CI
2		2B	RSC WG			2C	NISQ
6						6D	RU WZ
8		8XP10	WS			RAD	WB

Table 4-XXIII. Subinstruction TC0

Time	BR1 and BR2	Involuntary		TC0		IC3	
		XP	CP	XP	CP	XP	CP
1				1D	RB	1A	WY12 CI
2		2B	RSC WG			2C	NISQ
3				3XP6	RZ WQ		
6						6D	RU WZ
8		8XP10	WS			RAD	WB

Table 4-XXIV. Subinstruction TCF0

Time	BR1 and BR2	Involuntary		TCF0		IC3	
		XP	CP	XP	CP	XP	CP
1				1D	RB	1A	WY12 C1
2		2B	RSC WG			2C	N1SQ
6						6D	RU WZ
8		8XP10	WS			RAD	WB

Table 4-XXV. Subinstruction TCSAJ3

Time	BR1 and BR2	Involuntary		TCSAJ3	
		XP	CP	XP	CP
2		2B	RSC WG		
8		8XP10	WS	8E	WZ ST2

Table 4-XXVI. Subinstruction GOJ1

Time	BR1 and BR2	Involuntary		GOJ1	
		XP	CP	XP	CP
2		2B	RSC WG		
8		8XP10	WS	8D RSTRT	WB

Table 4-XXVII. Subinstruction DAS0

Time	BR1 and BR2	Involuntary		DAS0		IC10	
		XP	CP	XP	CP	XP	CP
1				RL10BB	WS	1A 1B	CI WY12 MONEX
2		2B	RSC WG				
3				3F	RA WB		
4				4H	RL WA		
5				5XP12	RU WL		
6				6B	A2X RG WY		
7				7B 7G	RB WA		
8		⚠1		8D 8XP12	WB RL		
9				9XP5	RU TOV WG WSC		
10	XX			10C	RA WY	10XP1	ST1
10	01			10XP8	PONEX		
10	10			10XP7	MONEX		
11				11E	RU WA		

⚠1 Crosspoint pulse 8XP10 is inhibited by command signal DAS0.

Table 4-XXVIII. Subinstruction DAS1

Time	BR1 and BR2	Involuntary		DAS1	
		XP	CP	XP	CP
1				RL10BB	WS
2		2B	RSC WG		
5				5K 5L	RG A2X WY
6				6XP8	RU TOV WG WSC
7	XX			7G	WA
7	01			7XP10	RB1
7	10			7XP11	R1C
8		8XP10	WS	8XP4	RZ ST2
9				9M	RC TMZ
10	X0			10E	WL
11	01			11E	RU WA

Table 4-XXIX. Subinstruction LXCH0

Time	BR1 and BR2	Involuntary		IC8		IC9	
		XP	CP	XP	CP	XP	CP
1						RL10BB	WS
2		2B	RSC WG				
3				3G	RL WB		
5				5XP13	RG WL		
7						7J	RB WG WSC
8		8XP10	WS			8XP4	RZ ST2

Table 4-XXX. Subinstruction INCR0

Time	BR1 and BR2	Involuntary		INCR0		PRINC	
		XP	CP	XP	CP	XP	CP
1						RL10BB	WS
2		2B	RSC WG				
5						5G 5L	RG TMZ TPZG TSGN WY
6				6XP10	PONEX		
7						7H WOVR	RU WG WSC
8		8XP10	WS			8XP4	RZ ST2

Table 4-XXXI. Subinstruction ADS0

Time	BR1 and BR2	Involuntary		ADS0		DAS1	
		XP	CP	XP	CP	XP	CP
1						RL10BB	WS
2		2B	RSC WG				
5						5K 5L	RG A2X WY
6						6XP8	RU TOV WG WSC
7	XX					7G	WA
7	01					7XP10	RB1
7	10					7XP11	R1C
8		8XP10	WS			8XP4	RZ ST2
9						9M	RC TMZ
11	XX			11E	RU WA		
11	01					11E	RU WA

Table 4-XXXII. Subinstructions CA0 and DCA1

Time	BR1 and BR2	Involuntary		IC6		IC13	
		XP	CP	XP	CP	XP	CP
2		2B	RSC WG				
7						7F	RG WB
8		8XP10	WS	8XP4	RZ ST2		
9						9B	RB WG
10				10XP9 10F	RB WA		

Table 4-XXXIII. Subinstructions CS0 and DCS1

Time	BR1 and BR2	Involuntary		IC7		IC13	
		XP	CP	XP	CP	XP	CP
2		2B	RSC WG				
7						7F	RG WB
8		8XP10	WS	8XP4	RZ ST2		
9						9B	RB WG
10				10G 10F	RC WA		

Table 4-XXXIV. Subinstruction NDX0

Time	BR1 and BR2	Involuntary		NDX0		IC1		IC13	
		XP	CP	XP	CP	XP	CP	XP	CP
2		2B	RSC WG						
5				TRSM					
7								7F	RG WB
8		8XP10	WS			8XP3	RZ		
9								9B	RB WG
10						10XP1	ST1		

Table 4-XXXV. Subinstruction RSM3

Time	BR1 and BR2	Involuntary		RSM3	
		XP	CP	XP	CP
1				R15	
2		2B	RSC WG	2C	NISQ
5				5XP4	RG WZ
6				6A	RB WG
8		8XP10	WS	RAD	WB

Table 4-XXXVI. Subinstruction NDX1

Time	BR1 and BR2	Involuntary		IC2	
		XP	CP	XP	CP
1				1A 1C	WY12 CI RZ
2		2B	RSC WG	2C	NISQ
3				3XP5	RB WZ
4				4F 4L	RA WB
5				5H 5S	RZ WA
6				6D	RU WZ
7				7C	A2X RG WY
8		8XP10	WS	8C	RU
9				9H	RB WA
10				10D	RU WB

Table 4-XXXVII. Subinstruction XCH0

Time	BR1 and BR2	Involuntary		IC5		IC9	
		XP	CP	XP	CP	XP	CP
1						RL10BB	WS
2		2B	RSC WG				
3				3F	RA WB		
5				5Q 5S	RG WA		
7						7J	RB WG WSC
8		8XP10	WS			8XP4	RZ ST2

Table 4-XXXVIII. Subinstruction DXCH0

Time	BR1 and BR2	Involuntary		DXCH0		IC8		IC10	
		XP	CP	XP	CP	XP	CP	XP	CP
1				RL10BB	WS			1A 1B	WY12 CI MONEX
2		2B	RSC WG						
3						3G	RL WB		
5						5XP13	RG WL		
7				7J	RB WG WSC				
8		8XP10	WS	8C 8D	RU WB				
10								10XP1	ST1

Table 4-XXXIX. Subinstruction DXCH1

Time	BR1 and BR2	Involuntary		IC5		IC9	
		XP	CP	XP	CP	XP	CP
1						RL10BB	WS
2		2B	RSC WG				
3				3F	RA WB		
5				5Q 5S	RG WA		
7						7J	RB WG WSC
8		8XP10	WS			8XP4	RZ ST2

Table 4-XL. Subinstruction TS0

Time	BR1 and BR2	Involuntary		TS0		IC9	
		XP	CP	XP	CP	XP	CP
1						RL10BB	WS
2		2B	RSC WG				
3				3XP2 3F	TOV RA WB		
4	XX			4XP5	RZ WY12		
4	01			4A	CI L16		
4	10			4A	CI L16		
5	01			5E 5S	RB1 WA		
5	10			5F 5S	R1C WA		
6				6D	RU WZ		
7						7J	RB WG WSC
8		8XP10	WS			8XP4	RZ ST2

Table 4-XLI. Subinstruction AD0

Time	BR1 and BR2	Involuntary		AD0		IC11		IC13	
		XP	CP	XP	CP	XP	CP	XP	CP
2		2B	RSC WG						
7								7F	RG WB
8		8XP10	WS			8XP4	RZ ST2		
9								9B	RB WG
10				10XP9	RB	10XP10	A2X WY		
11						11E	RU WA		

Table 4-XLII. Subinstruction MASK0

Time	BR1 and BR2	Involuntary		MASK0		IC14	
		XP	CP	XP	CP	XP	CP
2		2B	RSC WG				
3				3F	RA WB		
4				4J	RC WA		
7						7F	RG WB
8		8XP10	WS	8XP4	RZ ST2		
9				9J	RA RC WY		
10						10D	RU WB
11				11B	RC	11C	WA

Table 4-XLIII. Subinstruction BZF0

Time	BR1 and BR2	Involuntary		IC15		IC16		IC17	
		XP	CP	XP	CP	XP	CP	XP	CP
2		2B	RSC WG						
3				3E	RA TMZ TSGN WG				
4				4G	TPZG				
5	X1	⚠1				5N	RB WY12 CI		
6	X1					6D	RU WZ		
8	XX	8XP10	WS						
8	X1					RAD 8XP15	WB NISQ		
8	X0	⚠2						8XP4	RZ ST2

⚠1 Branch condition X1 produces command IC16.

⚠2 Branch condition X0 produces command IC17.

Table 4-XLIV. Subinstruction MSU0

Time	BR1 and BR2	Involuntary XP	Involuntary CP	MSU0 XP	MSU0 CP	IC12 XP	IC12 CP
1						RL10BB	WS
2		2B	RSC WG				
5						5J	RG WB
6				6C	A2X CI RC WY		
7				7XP9 7G	RUS TSGN WA		
8		8XP10	WS	8XP4	RZ ST2		
9						9B	RB WG
10	1X			10C 10XP7	RA WY MONEX		
11				11XP2 11C	RUS WA		

Table 4-XLV. Subinstruction QXCH0

Time	BR1 and BR2	Involuntary		QXCH0		IC9	
		XP	CP	XP	CP	XP	CP
1						RL10BB	WS
2		2B	RSC WG				
3				RQ	WB		
5				5XP15	RG WQ		
7						7J	RB WG WSC
8		8XP10	WS			8XP4	RZ ST2

Table 4-XLVI. Subinstruction AUG0

Time	BR1 and BR2	Involuntary		AUG0		PRINC	
		XP	CP	XP	CP	XP	CP
1						RL10BB	WS
2		2B	RSC WG				
5						5G 5L	RG TMZ TPZG TSGN WY
6	0X			6XP10	PONEX		
6	1X			6E	MONEX		
7						7H WOVR	RU WG WSC
8		8XP10	WS			8XP4	RZ ST2

Table 4-XLVII. Subinstruction DIM0

Time	BR1 and BR2	Involuntary		DIM0		PRINC	
		XP	CP	XP	CP	XP	CP
1						RL10BB	WS
2		2B	RSC WG				
5						5G 5L	RG TMZ TPZG TSGN WY
6	00			6E	MONEX		
6	10			6XP10	PONEX		
7						7H WOVR	RU WG WSC
8		8XP10	WS			8XP4	RZ ST2

Table 4-XLVIII. Subinstruction DCA0

Time	BR1 and BR2	Involuntary		DCA0		IC4		IC10		IC13	
		XP	CP	XP	CP	XP	CP	XP	CP	XP	CP
1						1D	RB	1A 1B	CI WY12 MONEX		
2		2B	RSC WG								
7										7F	RG WB
8		8XP10	WS			8C	RU				
9										9B	RB WG
10				10XP9	RB	10E	WL	10XP1	ST1		

Table 4-XLIX. Subinstruction DCS0

Time	BR1 and BR2	Involuntary		DCS0		IC4		IC10		IC13	
		XP	CP	XP	CP	XP	CP	XP	CP	XP	CP
1						1D	RB	1A 1B	CI WY12 MONEX		
2		2B	RSC WG								
7										7F	RG WB
8		8XP10	WS			8C	RU				
9										9B	RB WG
10				10G	RC	10E	WL	10XP1	ST1		

Table 4-L. Subinstruction SU0

Time	BR1 and BR2	Involuntary XP	Involuntary CP	SU0 XP	SU0 CP	IC11 XP	IC11 CP	IC13 XP	IC13 CP
2		2B	RSC WG						
7								7F	RG WB
8		8XP10	WS			8XP4	RZ ST2		
9								9B	RB WG
10				10G	RC	10XP10	A2X WY		
11						11E	RU WA		

Table 4-LI. Subinstruction NDXX0

Time	BR1 and BR2	Involuntary XP	Involuntary CP	IC1 XP	IC1 CP	IC13 XP	IC13 CP
2		2B	RSC WG				
7						7F	RG WB
8		8XP10	WS	8XP3	RZ		
9						9B	RB WG
10				10XP1	ST1		

Table 4-LII. Subinstruction NDXX1

Time	BR1 and BR2	Involuntary		NDXX1		IC2	
		XP	CP	XP	CP	XP	CP
1						1A 1C	WY12 CI RZ
2		2B	RSC WG			2C	NISQ
3						3XP5	RB WZ
4						4F 4L	RA WB
5						5H 5S	RZ WA
6						6D	RU WZ
7						7C	A2X RG WY
8		8XP10	WS			8C	RU
9						9H	RB WA
10				EXT		10D	RU WB

Table 4-LIII. Subinstruction BZMF0

Time	BR1 and BR2	Involuntary		IC15		IC16		IC17	
		XP	CP	XP	CP	XP	CP	XP	CP
2		2B	RSC WG						
3				3E	RA TMZ TSGN WG				
4				4G	TPZG				
5	X1	△1				5N	RB WY12 CI		
5	1X					5N	RB WY12 CI		
6	X1					6D	RU WZ		
6	1X					6D	RU WZ		
8	X1					RAD 8XP15	WB NISQ		
8	1X					RAD 8XP15	WB NISQ		
8	00	△2						8XP4	RZ ST2
8	XX	8XP10	WS						

△1 Branch condition X1 or 1X produces command IC16.

△2 Branch condition 00 produces command IC17.

Table 4-LIV. Subinstruction READ0

Time	BR1 and BR2	Involuntary		READ0		INOUT	
		XP	CP	XP	CP	XP	CP
1					RL10BB	WS	
2		△1			2XP3	RA WB	
3					3D	WY	
4					4XP11 4L	RCH WB	
5				5A 5S	RB WA	△2	
6						6XP2	RA WB
8		8XP10	WS			8XP4	RZ ST2

△1 Crosspoint pulse 2B is inhibited by command INOUT.

△2 Crosspoint pulse 5XP11 is inhibited by command READ0.

Table 4-LV. Subinstruction WRITE0

Time	BR1 and BR2	Involuntary		WRITE0		INOUT	
		XP	CP	XP	CP	XP	CP
1						RL10BB	WS
2		⚠1		2A	WG	2XP3	RA WB
3						3D	WY
4						4XP11 4L	RCH WB
5				5B	RA WCH	⚠2	
6						6XP2	RA WB
8		8XP10	WS			8XP4	RZ ST2

⚠1 Crosspoint pulse 2B is inhibited by command INOUT.

⚠2 Crosspoint pulse 5XP11 is inhibited by command WRITE0.

Table 4-LVI. Subinstruction RAND0

Time	BR1 and BR2	Involuntary		RAND0		INOUT	
		XP	CP	XP	CP	XP	CP
1						RL10BB	WS
2		△1				2XP3	RA WB
3				3B	RC	3D	WY
4						4XP11 4L	RCH WB
5				5R	RC	5XP11	RU WA
6						6XP2	RA WB
7				7XP7	RC WA		
8		8XP10	WS			8XP4	RZ ST2

△1 Crosspoint pulse 2B is inhibited by command INOUT.

Table 4-LVII. Subinstruction WAND0

Time	BR1 and BR2	Involuntary		WAND0		INOUT	
		XP	CP	XP	CP	XP	CP
1						RL10BB	WS
2		△1				2XP3	RA WB
3				3B	RC	3D	WY
4						4XP11 4L	RCH WB
5				5R	RC	5XP11	RU WA
6						6XP2	RA WB
7				7XP7 7XP14	RC WA WCH		
8		8XP10	WS			8XP4	RZ ST2

△1 Crosspoint pulse 2B is inhibited by command INOUT.

Table 4-LVIII. Subinstruction ROR0

Time	BR1 and BR2	Involuntary		ROR0		INOUT	
		XP	CP	XP	CP	XP	CP
1						RL10BB	WS
2		⚠1				2XP3	RA WB
3				3A	RB	3D	WY
4						4XP11 4L	RCH WB
5				5XP19	RB	5XP11	RU WA
6						6XP2	RA WB
8		8XP10	WS			8XP4	RZ ST2

⚠1 Crosspoint pulse 2B is inhibited by command INOUT.

Table 4-LIX. Subinstruction WOR0

Time	BR1 and BR2	Involuntary		WOR0		INOUT	
		XP	CP	XP	CP	XP	CP
1						RL10BB	WS
2		⚠1				2XP3	RA WB
3				3A	RB	3D	WY
4						4XP11	RCH WB
5				5C 5XP19	WCH RB	5XP11	RU WA
6						6XP2	RA WB
8		8XP10	WS			8XP4	RZ ST2

⚠1 Crosspoint pulse 2B is inhibited by command INOUT.

Table 4-LX. Subinstruction RXOR0

Time	BR1 and BR2	Involuntary		RXOR0		INOUT		IC14	
		XP	CP	XP	CP	XP	CP	XP	CP
1						RL10BB	WS		
2		[1]				2XP3	RA WB		
3				3XP7	RC RCH	3D	WY		
4						4XP11 4L	RCH WB		
5				5D	RA RC WG	[2]			
7								7F	RG WB
8		8XP10	WS			8XP4	RZ ST2		
9				9A	RC WG				
10								10D	RU WB
11				11D	RC RG			11C	WA

[1] Crosspoint pulse 2B is inhibited by command INOUT.
[2] Crosspoint pulses 5XP11 and 6XP2 are inhibited by command RXOR0.

Table 4-LXI. Subinstruction RUPT0

Time	BR1 and BR2	Involuntary		RUPT0	
		XP	CP	XP	CP
1				R15	WS
2		2B	RSC WG		
9		△1		9XP1	RZ WG
10				10XP1	ST1

△1 Crosspoint pulse 8XP10 is inhibited by command RUPT0.

Table 4-LXII. Subinstruction RUPT1

Time	BR1 and BR2	Involuntary		RUPT1	
		XP	CP	XP	CP
1				R15 RB2	WS
2		2B	RSC WG		
3				RRPA	WZ
8		8XP10	WS	8XP4	RZ ST2
9				9B KRPT	RB WG

Table 4-LXIII. Subinstruction PINC

Time	BR1 and BR2	Involuntary		PINC		PARTC		INKL	
		XP	CP	XP	CP	XP	CP	XP	CP
1								RSCT	WS
2		2B	RSC WG						
5						5G 5L	RG TMZ TPZG TSGN WY		
6				6XP10	PONEX				
7				7H	RU			WOVR	WG WSC
8		8XP10	WS					8B	RB

Table 4-LXIV. Subinstruction MINC

Time	BR1 and BR2	Involuntary		MINC		PARTC		INKL	
		XP	CP	XP	CP	XP	CP	XP	CP
1								RSCT	WS
2		2B	RSC WG						
5						5G 5L	RG TMZ TPZG TSGN WY		
6				6E	MONEX				
7				7H	RU			WOVR	WG WSC
8		8XP10	WS					8B	RB

Table 4-LXV. Subinstruction PCDU

Time	BR1 and BR2	Involuntary		PCDU		PARTC		INKL	
		XP	CP	XP	CP	XP	CP	XP	CP
1								RSCT	WS
2		2B	RSC WG						
5						5G 5L	RG TMZ TPZG TSGN WY		
6				6XP12	CI				
7				7XP15	RUS			WOVR	WG WSC
8		8XP10	WS					8B	RB

Table 4-LXVI. Subinstruction MCDU

Time	BR1 and BR2	Involuntary		MCDU		PARTC		INKL	
		XP	CP	XP	CP	XP	CP	XP	CP
1								RSCT	WS
2		2B	RSC WG						
5						5G 5L	RG TMZ TPZG TSGN WY		
6				6E 6XP12	MONEX CI				
7				7XP15	RUS			WOVR	WG WSC
8		8XP10	WS					8B	RB

Table 4-LXVII. Subinstruction DINC

Time	BR1 and BR2	Involuntary		DINC		PARTC		INKL	
		XP	CP	XP	CP	XP	CP	XP	CP
1								RSCT	WS
2		2B	RSC WG						
5						5G 5L	RG TMZ TPZG TSGN WY		
6	00		△1	POUT 6E	 MONEX				
6	10			MOUT 6XP10	 PONEX				
6	X1			ZOUT					
7				7H	RU			WOVR	WG WSC
8		8XP10	WS					8B	RB

△1 Crosspoint pulses POUT, MOUT, and ZOUT are three (3) microseconds long, starting at time period T06 and ending with time period T08.

Table 4-LXVIII. Subinstruction SHINC

Time	BR1 and BR2	Involuntary XP	Involuntary CP	SHIFT XP	SHIFT CP	INKL XP	INKL CP
1						RSCT	WS
2		2B	RSC WG				
5				5XP9	RG TSGN WYD		
7						WOVR	WG WSC
8		8XP10	WS			8B	RB

Table 4-LXIX. Subinstruction SHANC

Time	BR1 and BR2	Involuntary XP	Involuntary CP	SHANC XP	SHANC CP	SHIFT XP	SHIFT CP	INKL XP	INKL CP
1								RSCT	WS
2		2B	RSC WG						
5				5M	CI	5XP9	RG TSGN WYD		
7								WOVR	WG WSC
8		8XP10	WS					8B	RB

Table 4-LXX. Subinstruction INOTRD

Time	BR1 and BR2	Involuntary		CHINC		INKL	
		XP	CP	XP	CP	XP	CP
1				1E	WS	△1	
2		2B	RSC WG				
5				5XP21	RCH		
8		8XP10	WS			8B	RB

△1 Crosspoint pulses RSCT and WOVR are inhibited by command MON+CH.

Table 4-LXXI. Subinstruction INOTLD

Time	BR1 and BR2	Involuntary		INOTLD		CHINC		INKL	
		XP	CP	XP	CP	XP	CP	XP	CP
1						1E	WS	△1	
2		2B	RSC WG						
5						5XP21	RCH		
7				7XP14	WCH				
8		8XP10	WS					8B	RB

△1 Crosspoint pulses RSCT and WOVR are inhibited by command MON+CH.

Table 4-LXXII. Subinstructions FETCH0 and STORE0

Time	BR1 and BR2	Involuntary		FETCH0		MON		INKL	
		XP	CP	XP	CP	XP	CP	XP	CP
1				R6	WS			△1	
2		2B	RSC WG	2XP8	ST1 WY				
4						4M	WSC		
8		8XP10	WS					△2	

△1 Crosspoint pulses RSCT and WOVR are inhibited by command MON+CH.

△2 Crosspoint pulse 8B is inhibited by command MON.

Table 4-LXXIII. Subinstruction FETCH1

Time	BR1 and BR2	Involuntary		MON		STFET1		INKL	
		XP	CP	XP	CP	XP	CP	XP	CP
2		2B	RSC WG	△1				△2	
7						7E	RG		
8		8XP10	WS			U2BBK	△3	8B	RB
10						RBBK			

△1 Crosspoint pulse 4M is inhibited by command FETCH1.

△2 Crosspoint pulses RSCT and WOVR are inhibited by command MON+CH.

△3 Crosspoint pulse U2BBK may be inhibited by signal MONWBK from the peripheral equipment.

Table 4-LXXIV. Subinstruction STORE1

Time	BR1 and BR2	Involuntary		MON		STFET1		STORE1		INKL	
		XP	CP	XP	CP	XP	CP	XP	CP	XP	CP
2		2B	RSC WG							(1)	
4				4M	WSC						
7						7E	RG				
8		8XP10	WS			U2BBK	(2)			8B	RB
9								9C	WG		
10						RBBK					

(1) Crosspoint pulses RSCT and WOVR are inhibited by command MON+CH.

(2) Crosspoint pulse U2BBK may be inhibited by signal MONWBK from the peripheral equipment.

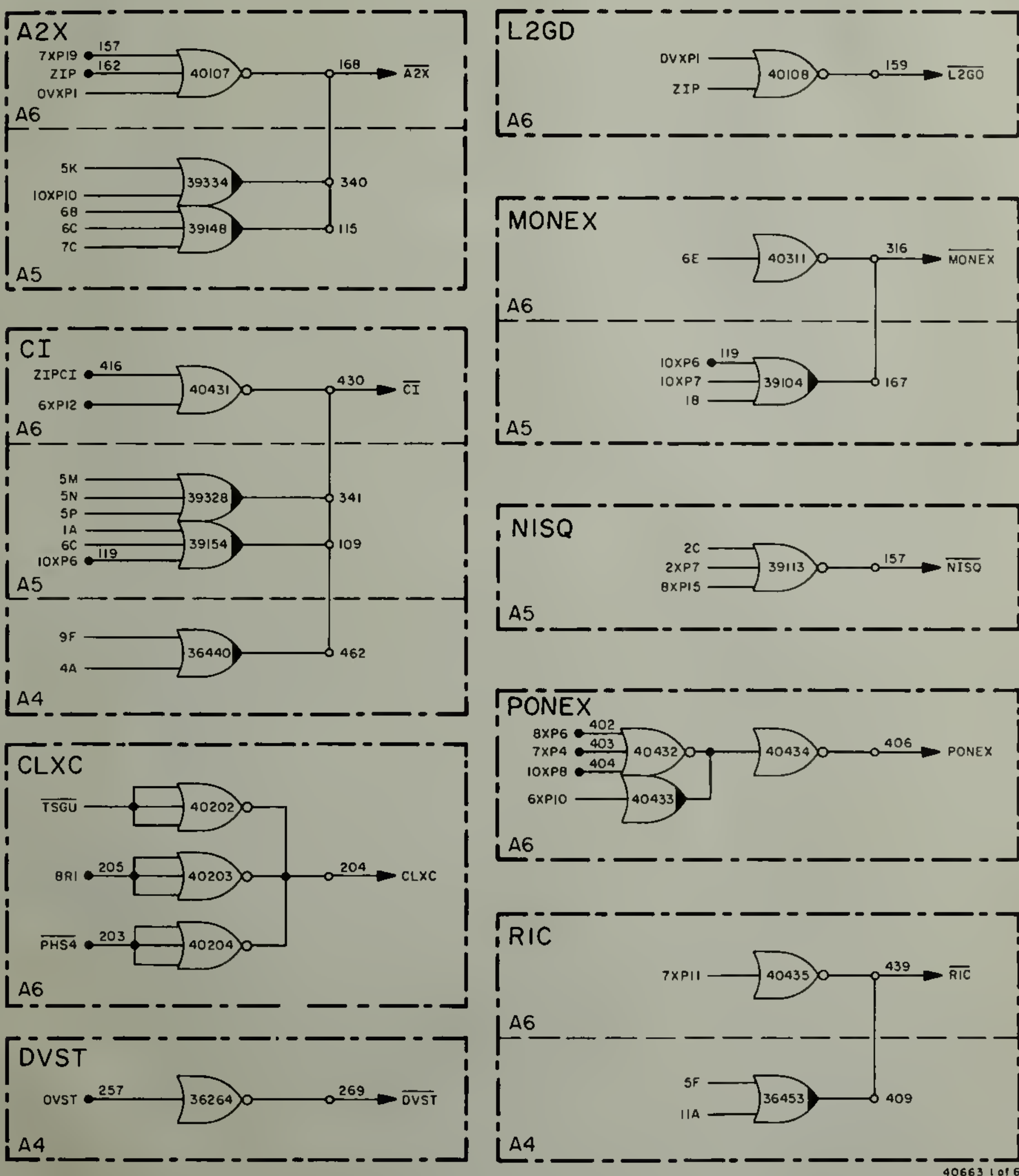


Figure 4-135. Control Pulse Gates, Logic Diagram (Sheet 1 of 6)

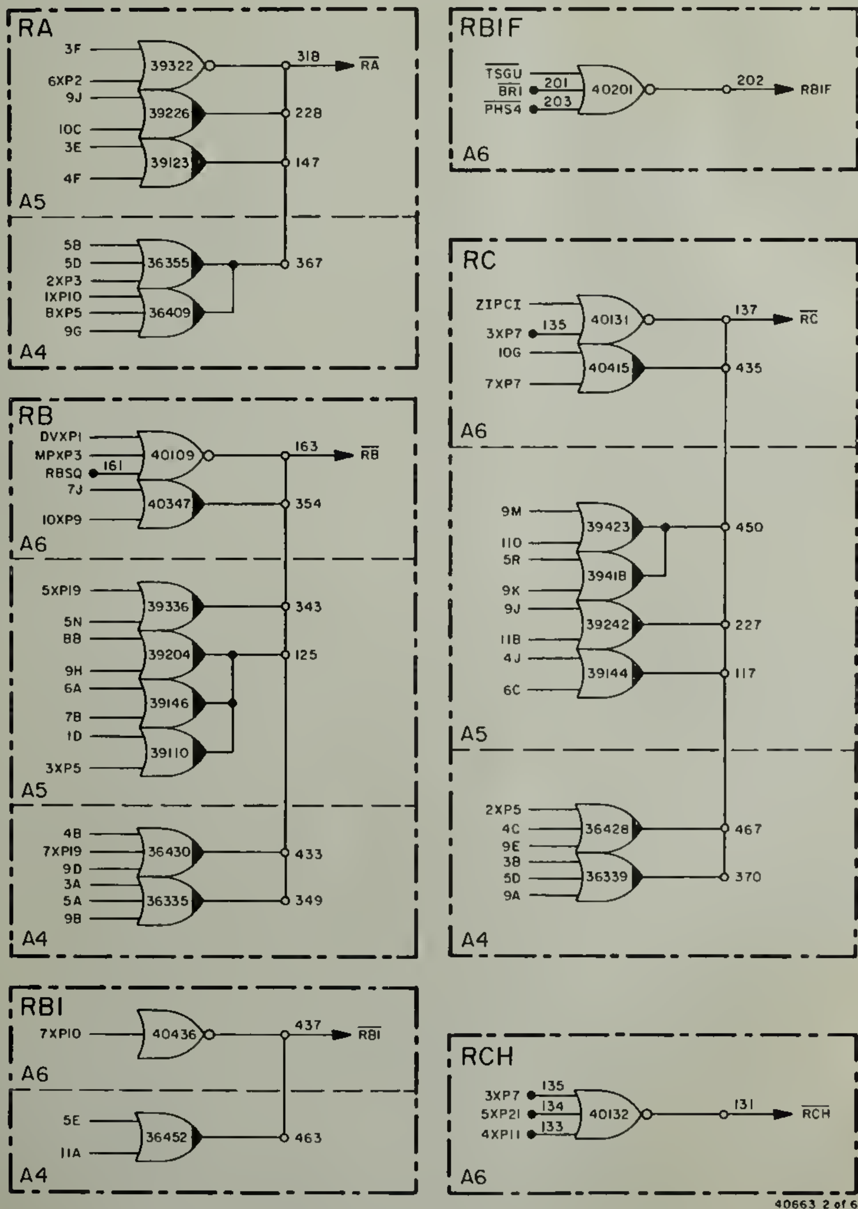


Figure 4-135. Control Pulse Gates, Logic Diagram (Sheet 2 of 6)

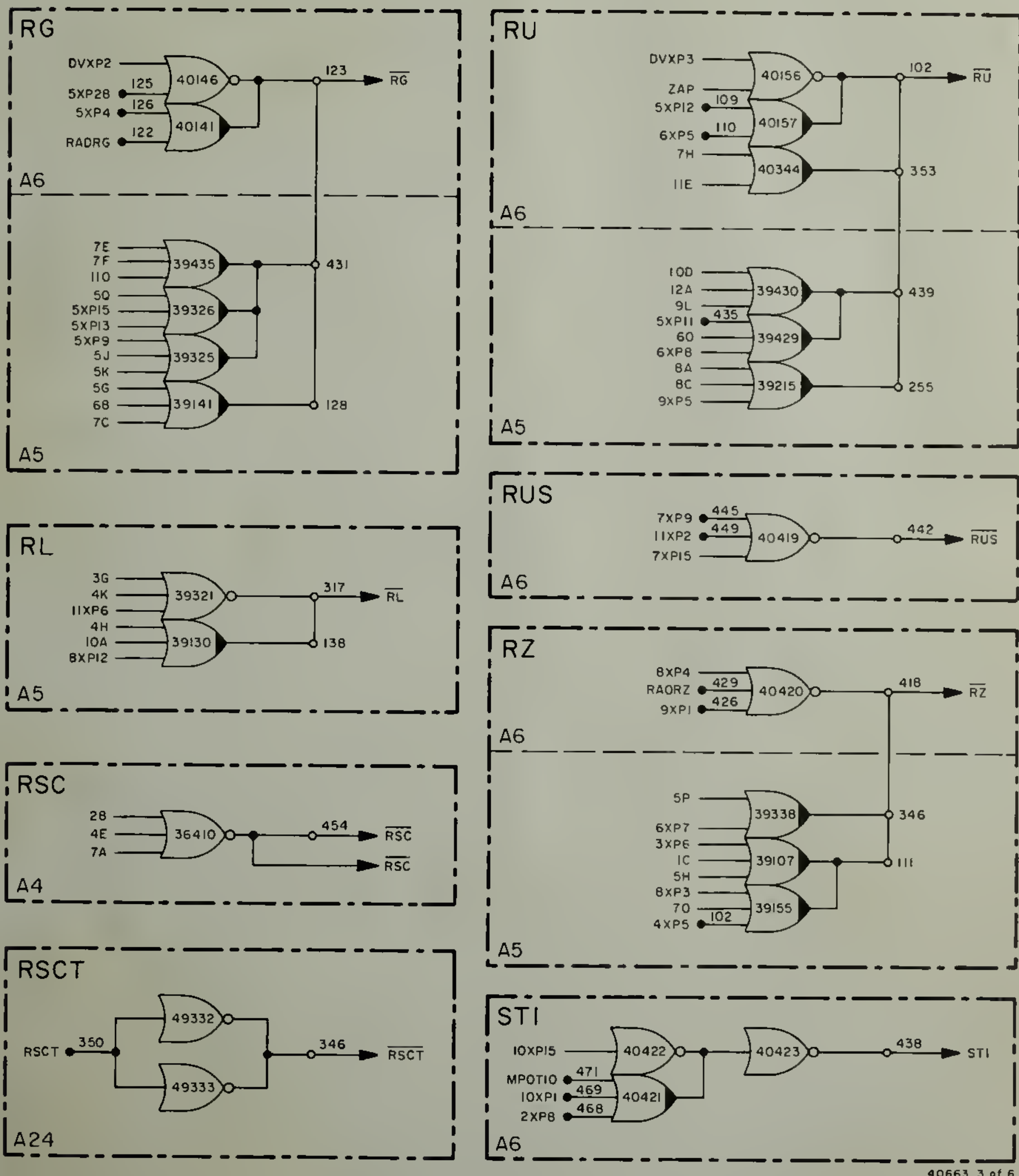


Figure 4-135. Control Pulse Gates, Logic Diagram (Sheet 3 of 6)

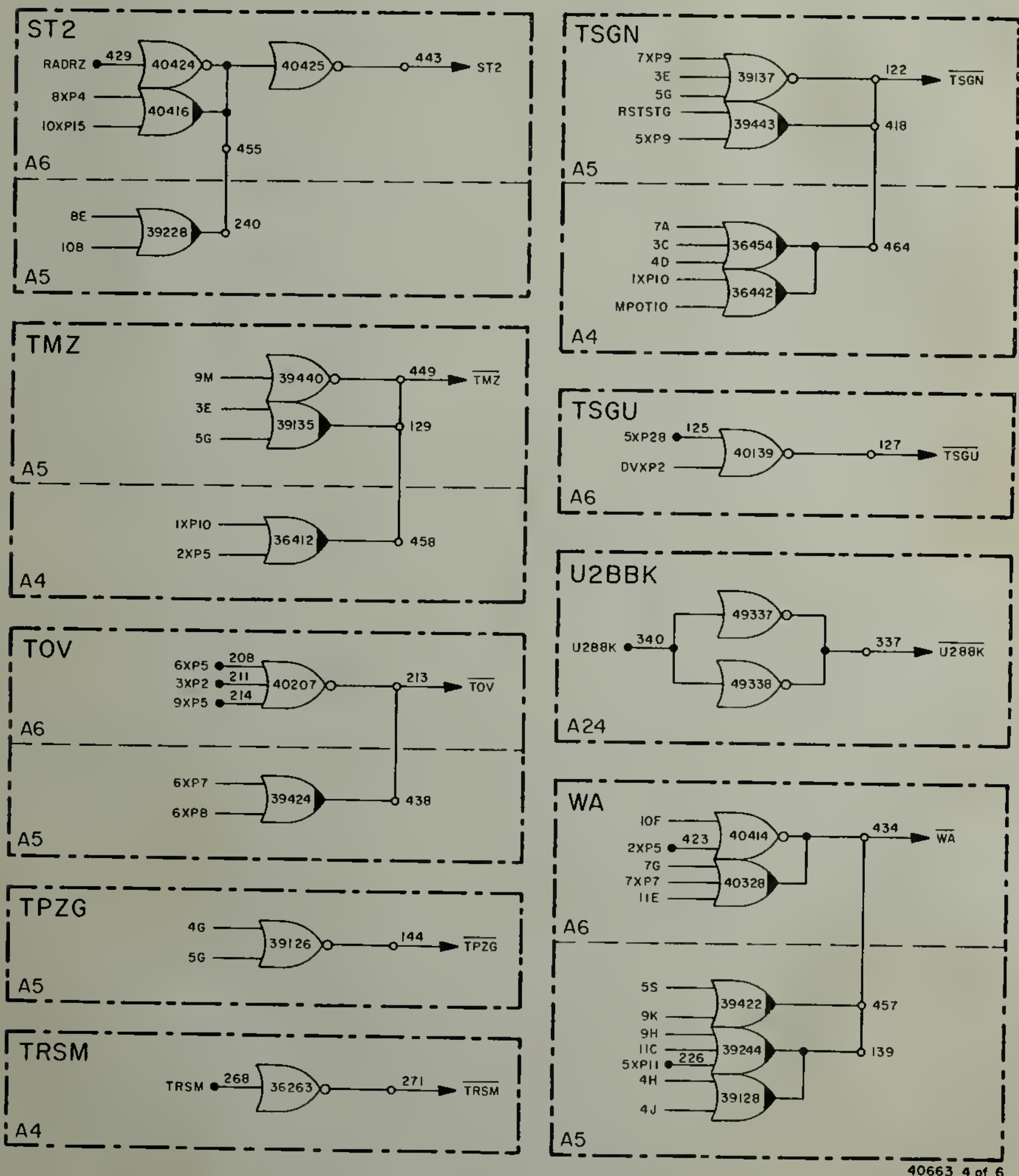


Figure 4-135. Control Pulse Gates, Logic Diagram (Sheet 4 of 6)

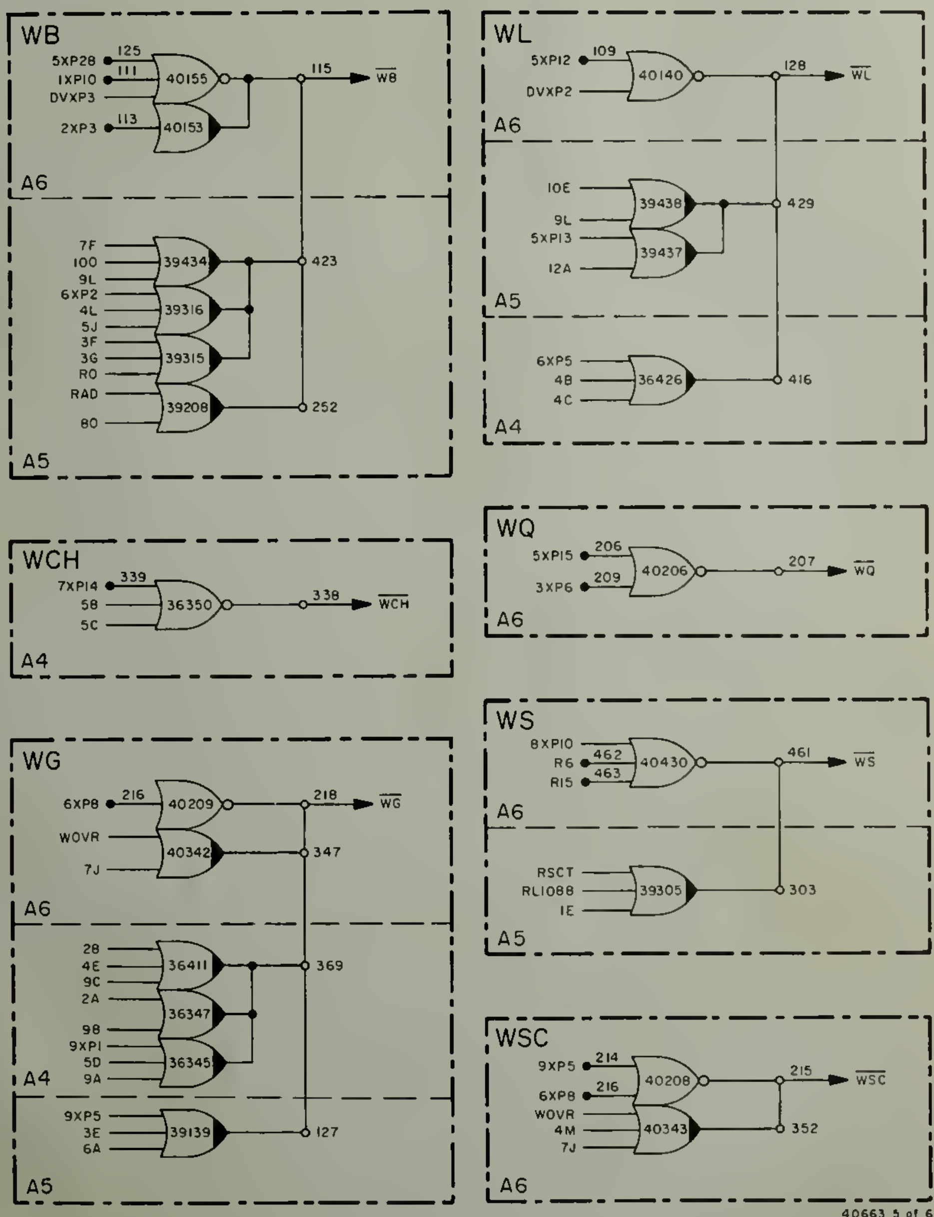


Figure 4-135. Control Pulse Gates, Logic Diagram (Sheet 5 of 6)

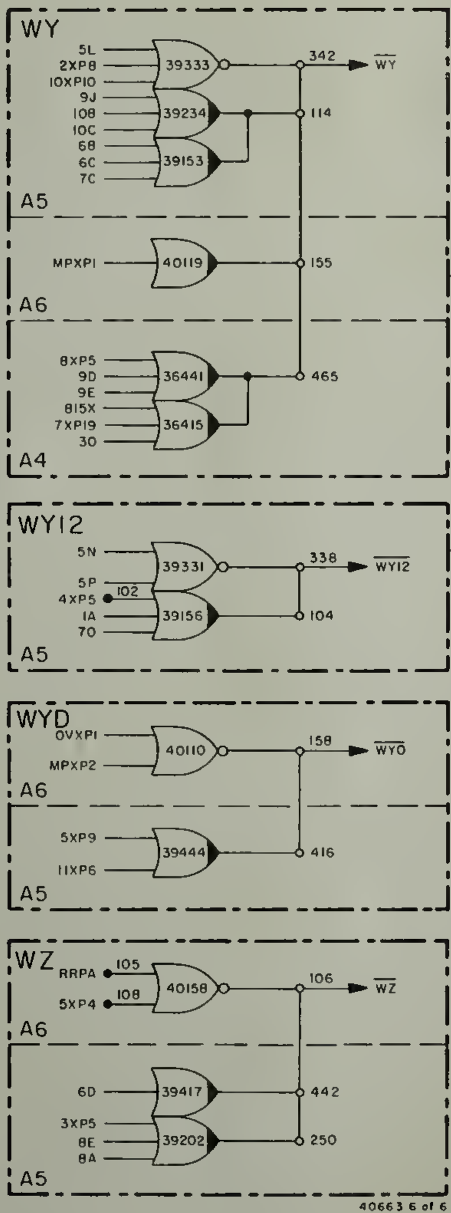


Figure 4-135. Control Pulse Gates, Logic Diagram (Sheet 6 of 6)

Table 4-LXXV. Control Pulse Origin

Circuit	Control Pulses
T01 crosspoint	R15 RB2 RL10BB
T03 crosspoint	RRPA RQ
T04 crosspoint	L16 (4A)
T05 crosspoint	B15X Z16
T06 crosspoint	TL15
T07 crosspoint	TSGN2 PTWOX WOVR
T08 crosspoint	RAD RSTRT RSTSTG Z15 (9K)
T09 crosspoint	KRPT
T10 crosspoint	EXT RBBK
Divide crosspoint	PIFL
Multiply crosspoint	MCR0 ZIP ZAP
Control pulse gates	A2X CI CLXC DVST L2GD MONEX
Control pulse gates (cont)	NISQ PONEX R1C RA RB RB1 RB1F RC RCH RG RL RSC RSCT RU RUS RZ ST1 ST2 TMZ TOV TPZG TRSM TSGN TSGU U2BBK WA WB WCH WG WL WQ WS WSC WY WY12 WYD WZ
L service	G2LS WALS

(Sheet 1 of 2)

Table 4-LXXV. Control Pulse Origin

Circuit	Control Pulses	Circuit	Control Pulses
Channel 14	POUT MOUT ZOUT	Register EB	REB WEB
Adder	NEACOF NEACON	Register FB	RFB WFB WBBK
Register SQ control	WSQ	Stage Counter	DIVSTG (STAGE)

(Sheet 2 of 2)

4-5.4.12 Branch Control. The branch control (figure 4-136) consists of the branch flip-flops, branch decoder, and special instruction flip-flop. The branch flip-flops and decoder control up to four different sets of control pulses at a given time during various subinstructions. The special instruction flip-flop controls two sets of control pulses at a given time depending on whether or not the next instruction to be executed is special instruction RELINT, INHINT, or EXTEND.

The branch 1 flip-flop is used to test the sign bit and the negative overflow bits of any word placed onto the write lines. It also tests bit 15 of register L and bit 16 of the adder. These tests are performed by control pulses TSGN, TOV, TL15, and TSGU, respectively. The test control pulses are similar to write control pulses in that they are used to clear the flip-flop register before or during the write process. As a result, the output of the branch flip-flops cannot be used until the final state is established. Normally all control pulses produced from a branch condition occur one or more time periods after the test control pulses. For examplc, test control pulse TOV of subinstruction TS0 will establish a new state for the branch flip-flops at time pulse T03. The control pulscs resulting from the state of the branch flip-flops are produced at time pulses T04 and T05.

A special case exists for the divide instruction. Control pulse TSGU does not set or reset the branch 1 flip-flop in the normal manner. Bit position 16 of the adder is used as a primary level device with the branch 1 flip-flop being the secondary level device. Control pulse TSGU transfers bit 16 of the adder to the branch 1 flip-flop. If bit 16 is a logic ONE (signals SUMA16 and SUMB16 are present) and the branch 1 flip-flop is already set, no change of state occurs. Signal TSGU is gated by signal PHS3. Therefore, the final state of the branch flip-flop is established 1/4-microsecond before

BRANCH 1 FLIP-FLOP	
SIGNAL	EQUATION
SGUM	SUMA16 SUMB16 TSGU PHS3
A	UNF TOV
B	LIS TLIS
C	WL16 TSGN PHS4
D	TSGN PHS3
E	TL15 PHS3
F	$\overline{\text{SUMA15 SUMB16}}$ TSGU PHS3
G	TOV PHS2
BR1	SGUM + A $\overline{G}$ + B $\overline{E}$ + C + BR1 $\overline{D}$ $\overline{E}$ $\overline{F}$ $\overline{G}$

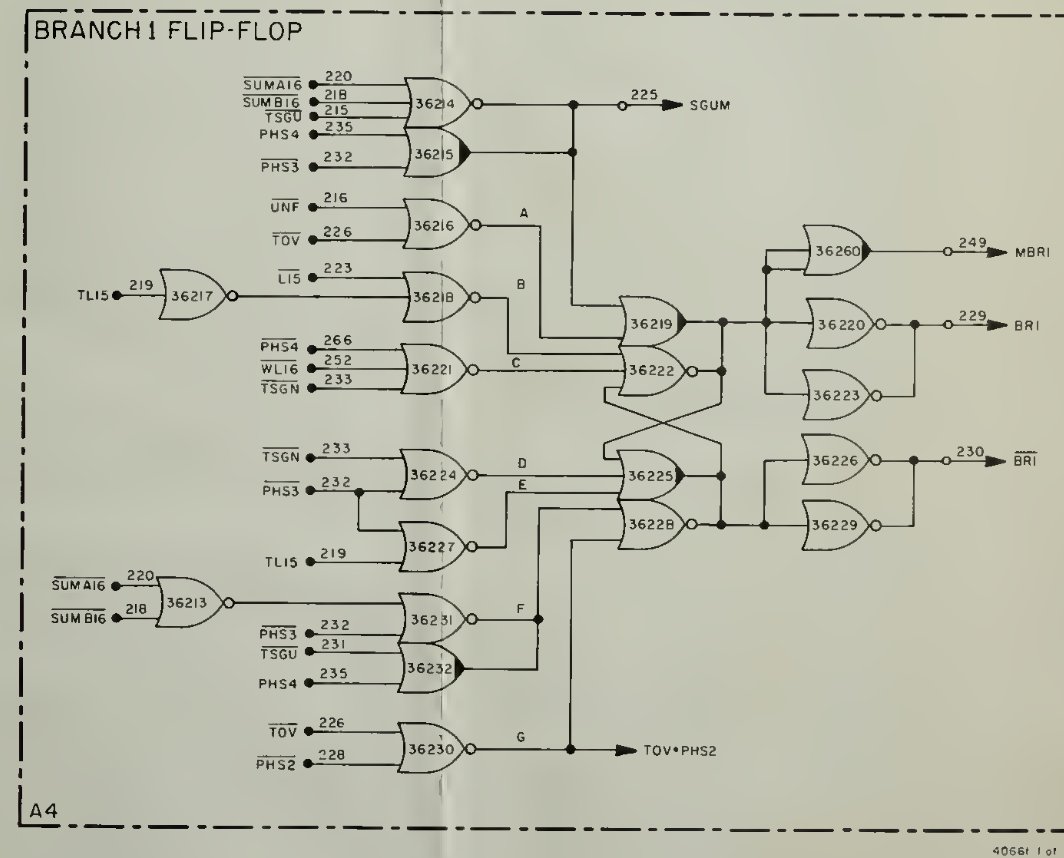
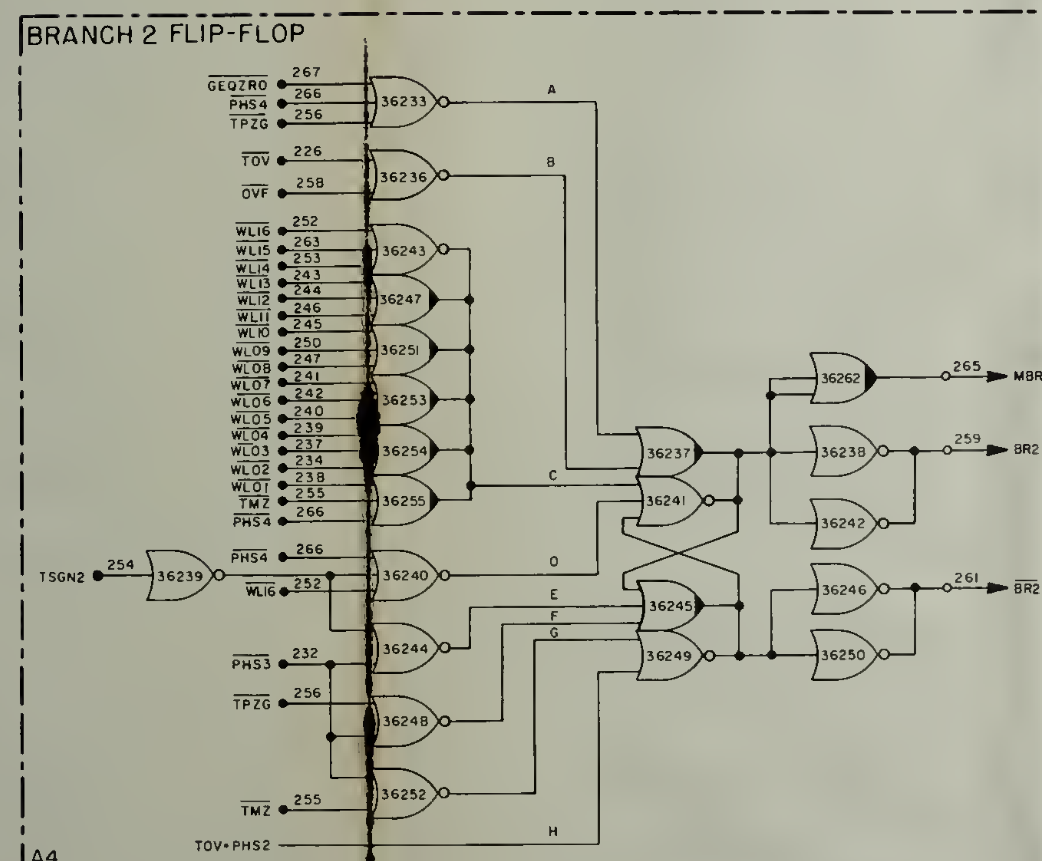
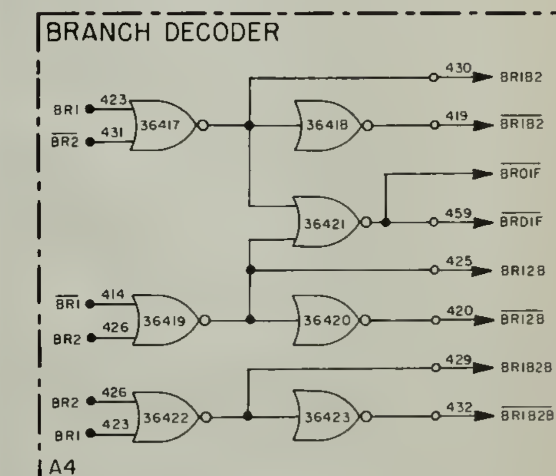


Figure 4-136. Branch Control, Logic Diagram (Sheet 1 of 3)

BRANCH 2 FLIP-FLOP	
SIGNAL	EQUATION
A	GEQZRO TPZG PHS4
B	OVF TOV
C	WL16 WL15 WL14 WL13 WL12 WL11 WL10 WL09 WL08 WL07 WL06 WL05 WL04 WL03 WL02 WL01 TMZ PHS3
D	WL16 TSGN2 PHS4
E	TSGN2 PHS3
F	TPZG PHS3
G	TMZ PHS3
H	TOV PHS2
BR2	A + B $\overline{\text{H}}$ + C + D + BR2 $\overline{\text{E}}$ $\overline{\text{F}}$ $\overline{\text{G}}$ $\overline{\text{H}}$





BRANCH DECODER	
SIGNAL	EQUATION
BR1B2	$\overline{\text{BR1}}$ BR2
BRDIF	$\overline{\text{BR1}}$ BR2 + BR1 $\overline{\text{BR2}}$
BR12B	BR1 $\overline{\text{BR2}}$
BR1B2B	$\overline{\text{BR1}}$ $\overline{\text{BR2}}$

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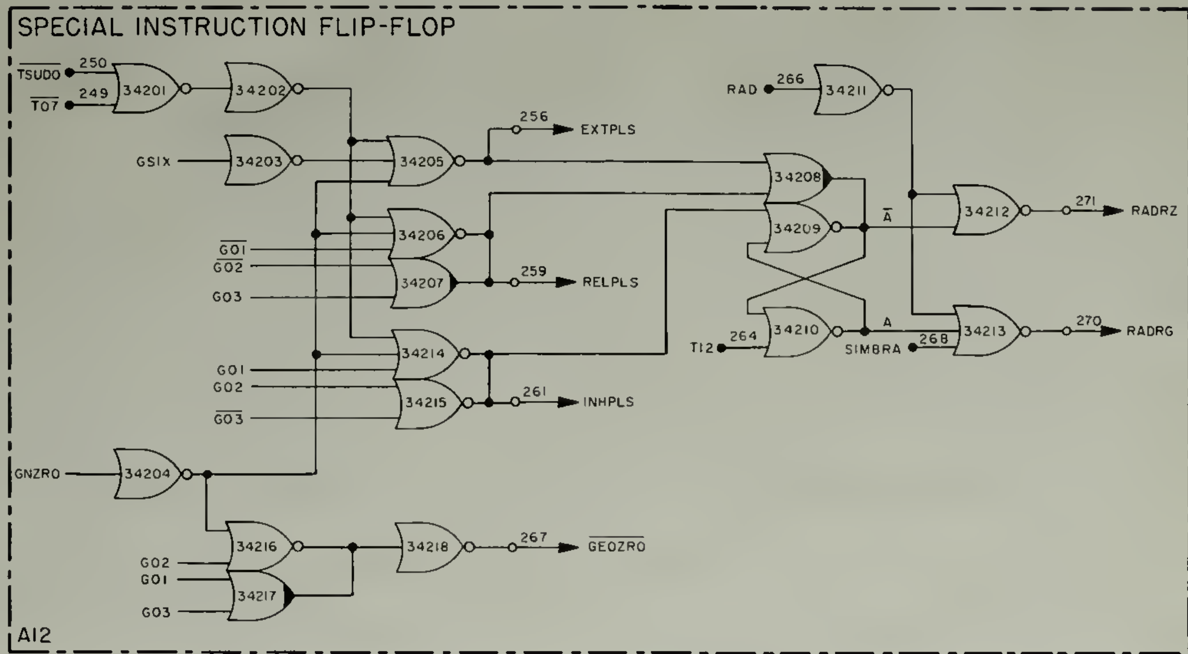
Figure 4-136. Branch Control, Logic Diagram (Sheet 2 of 3)



SPECIAL INSTRUCTION FLIP-FLOP	
SIGNAL	EQUATION
EXTPLS	T07 TSUDO GNZRO GSIX
RELPLS	T07 TSUDO GNZRO $\overline{G03}$ G02 G01
INHPLS	T07 TSUDO GNZRO G03 $\overline{G02}$ $\overline{G01}$
GEQZRO	GNZRO $\overline{G03}$ $\overline{G02}$ $\overline{G01}$
A	EXTPLS + RELPLS + INHPLS + A $\overline{T12}$
RADRZ	A RAD
RADRG	$\overline{A}$ RAD $\overline{SIMBRA}$

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Figure 4-136. Branch Control, Logic Diagram (Sheet 3 of 3)

control pulse TSGU ends. During this 1/4-microsecond interval, TSGU is gated by signal PHS4 and, in conjunction with the output of the branch 1 flip-flop, produces control pulse CLXC or RB1F. These control pulses are generated by the control pulse gates shown in figure 4-135.

Negative overflow exists when bits 16 and 15 of a word are logic ONE and ZERO, respectively. Negative overflow means that a large negative quantity has been produced in some manner and cannot be processed by the computer because of its limited word length. This condition is monitored during certain operations to prevent faulty computations. When negative overflow exists, a new branch state is established, and a set of control pulses designed to adjust computer operations are produced. The test is accomplished by control pulse TOV. This control pulse is gated by signal PHS2 to first clear the branch 1 and 2 flip-flops. At the same time control pulse TOV tests signal UNF. If signal UNF is present, the branch 1 flip-flop is set. Since the PHS2 signal occurs during the second 1/4-microsecond interval of a time period, the branch 1 flip-flop does not set until the third 1/4-microsecond period.

Control pulse TL15 tests bit 15 of register L. Control pulse TL15 is first gated by signal PHS3 to reset the branch 1 flip-flop and then by signal PHS4 to set the flip-flop if signal L15 is present.

Control pulse TSGN tests write line WL16 for sign. Control pulse TSGN is first gated by signal PHS3 to reset the branch 1 flip-flop and then by signal PHS4 to set the flip-flop if signal WL16 is present. Signal WL16 is present when the content placed onto the write lines is negative.

Signal BR1 is produced when the branch 1 flip-flop is set. Signal MBR1 is applied to an indicator on the peripheral equipment together with the output of the branch 2 flip-flop. In this manual the content of the two branch flip-flops are referred to as c(BR1, BR2) whereas the indicators on the peripheral equipment display c(BR2, BR1).

The branch 2 flip-flop is used to test plus zero, positive overflow, and minus zero. It is also used to test the sign of one quantity while the branch 1 flip-flop tests the sign of another quantity. It is necessary to determine the sign of two quantities being multiplied together in order to establish the correct sign of the product. The branch 2 flip-flop is always cleared before a net input occurs. Control pulse TPZG tests for plus zero in register G. Control pulse TPZG is first gated by signal PHS3 to clear the branch 2 flip-flop and then by signal PHS4 to set the flip-flop if signal GEQZRO is present.

Positive overflow exists when bits 16 and 15 of a word are 0 and 1, respectively. Positive overflow means that computer word length has been exceeded by a large positive quantity. Signal OVF is present when this condition exists. Control pulse TOV, which also tests negative overflow, is gated by signal PHS2 to clear both branch flip-flops. After the flip-flops are cleared, the branch 2 flip-flop will be set if signal TOV is present.

Control pulse TMZ detects a minus zero quantity placed onto write lines WL16 through WL01. Control pulse TMZ is first gated by signal PHS3 to clear the branch 2 flip-flop and then by signal PHS4 to set the flip-flop if minus zero exists.

Control pulse TSGN2 tests write line WL16 for positive and negative values. If signal WL16 is present, a negative quantity has been placed onto the write lines. Control pulse TSGN2 is first gated by signal PHS3 to clear the branch 2 flip-flop and then by signal PHS4 to set the flop-flop if signal WL16 is present.

Signal BR2 is produced when the branch 2 flip-flop is set. Signal MBR2 is sent to the peripheral equipment to indicate the state of the branch 2 flip-flop.

The outputs of the branch flip-flops are used by the crosspoint generator circuits to produce control pulses. In addition, the branch decoder circuit detects states 01, 01 or 10, 10, and 00, and produces signals BR1B2, BRD1F, BR12B, and BR1B2B, respectively.

The special instruction flip-flop is used to control RELINT, INHINT, and EXTEND instructions. These special instructions are address-dependent and identified by order codes 00.0003, 00.0004, and 00.0006, respectively. These order codes are never entered into register SQ. Instead, they are entered into register G and recognized when certain subinstructions are being executed. The subinstructions which recognize the special instruction order codes produce signal TSUD0. They are STD2, TC0, TCF0, RSM3, MP3, BZF0, and BZMF0. Each of these subinstructions fetch the next instruction to be executed. When doing so, signal TSUD0 and time pulse T07 are ANDed. The resulting crosspoint pulse tests the decoded output of register G for octal 3, 4, or 6 and produces signal RELPLS, INHPLS, or EXTPLS if the respective octal quantity is contained in register G. Flip-flop A is set by signal RELPLS, INHPLS, or EXTPLS at time pulse T07 and reset by time pulse T12. At time pulse T08 of these fetching subinstructions, control pulse RAD is produced by signals TSUD0 and T08 and converted into signal RADRZ if flip-flop A is set or into signal RADRG if the flip-flop is not set. Signal RADRZ is then converted into control pulses RZ and ST2 which cause subinstruction STD2 to be executed. Signal RADRG, produced when anything other than a special instruction is being fetched for execution, is then converted into control pulse RG which, in conjunction with control pulse WB, transfers the basic instruction word to the central processor register B. Signal EXTPLS which set flip-flop A and produces control pulses RZ and ST2 also sets the FUTEXT flip-flop in the register SQ circuit. Similiarly, signal INHPLS sets the INHINT flip-flop in the register SQ control and signal RELPLS resets the INHINT flip-flop.

4-5.5 CENTRAL PROCESSOR. The central processor performs all arithmetic operations required of the LGC, initiates the selection of and buffers all information coming from and going to memory, checks for correct parity on all words coming from memory, and generates parity for all words written into memory.

4-5.5.1 Central Processor Functional Description. The central processor consists of eight 16 bit flip-flop registers with service gates, a 12 bit memory address register and decoder, the write amplifiers and parity logic. The flip-flop registers to be discussed are special and central registers (A, Q, Z, and L) which are addressable, register B, the memory buffer register G, and registers X and Y which comprise the arithmetic unit or adder.

Data words and basic instruction words consist of 16 bits when stored in fixed or erasable memory. The word format is illustrated in figure 4-137. The formats presented in this illustration indicate the word as it actually appears in the hardware. The concept employed by programmers when indicating a data word or basic instruction word differs from that shown in figure 4-137.

An instruction word in memory (a) contains the operation code (OC) in bit positions 16, 14, and 13, parity (P) in bit position 15, and the data address (A) in bit positions 1 through 12. When the word is read out of memory, the parity bit is applied directly to

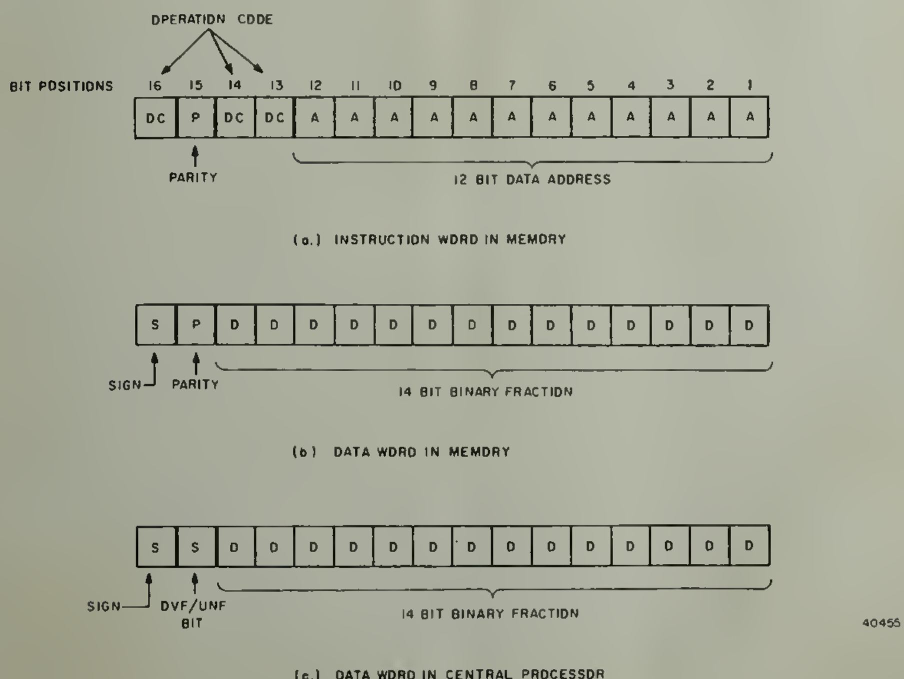

Figure 4-137. Word Formats

the parity logic. There is no other manipulation of the parity bit within the central processor. The word contains the same quantity in bit positions 15 and 16 when residing in the central processor. The operation code is applied to the sequence generator, and the 12 bit address to the memory address register. Program listings indicate the order of an instruction word using six octal bits as follows:

0 6501 0

The first bit (0) represents the operation code and includes bit positions 16, 14, and 13. The next four bits (6501) represent the relevant address of the instruction word in positions 12 through 1. The bit at the extreme right is the parity bit (position 15).

A data word in memory (b) contains the sign in bit position 16, parity in bit position 15, and the value bits in positions 14 through 1. When transferred to the central processor, the parity bit is again applied to the parity logic. A data word in the central processor (c), contains the sign entered into bit positions 15 and 16. Position 15 then becomes an indication of overflow or underflow. Program listings indicate the order of a data word using six octal bits as follows:

50106 0

The first octal bit (5, which is 101 in binary) includes bit positions 16, 14, and 13. In this case, the sign is minus indicating a negative number, and positions 14 and 13 are the two high order bits of the 14 bit binary fraction. The remaining 12 bits are represented by octal bits 0106. The parity bit is at the extreme right.

Each flip-flop register consists of 16 bit positions, which is consistent with the word format discussed previously. The register service gates control the write-in and read-out operations of each register. (See figure 4-138.) The bit positions are cleared coincident with write-in. Normally, data from the write lines is applied to the service gates, and is written into a particular register under control of a write control pulse from the sequence generator. For example, data from the write lines applied to register A service is written into register A coincident with write control pulse WA. Information in the register is read out by read control pulse RA. Data is exchanged between registers in this manner by reading out one register and writing into another simultaneously. Some of the flip-flop registers have additional conditions under which information is written in. Under program control, an associated address can be generated to write into and read out of each of these registers. Registers A, Q, Z, and L are addressable and are referred to as special and central registers.

Registers A (accumulator), L (low order product), Q, and X and Y (arithmetic unit or adder) are primarily involved in arithmetic operations. The adder processes two quantities; the quantity entered into Y and one of three quantities (+1, -1, +2) entered into X dependent on the instruction being executed. Registers Z and B are essentially storage elements in that they store the operation or step to be performed next in the program.

Register G is normally controlled by the service gates and control pulses WG and RG. However, under program control and coincident with an associated address, a word entered into register G is manipulated by the editing control section. Register G buffers all information read out of memory into the central processor, and buffers all information written into memory from the central processor. A word transferred from memory (SA01-SA16) as a result of selection through the memory address register is deposited directly into the bit positions of register G. The word is read out to the write lines under control of read pulse RG. A word being written into erasable memory (GEM01-GEM16) is buffered through G from the write lines by control pulse WG. Editing control allows a word entered into register G to be cycled or shifted (as a function of address) to accomplish specific program manipulations.

The parity bit (SAP) is entered into the parity logic on a read-out from memory, and is used to indicate correct parity. A parity alarm occurs in case of incorrect parity. There is no manipulation of the parity bit within the central processor. The parity logic also generates a parity bit (GEM15) when a word is written into erasable memory. Odd parity is used in the LGC; therefore, the total number of ONE's in the word including parity is odd.

The memory address register (S) accepts the 12 bit address contained in an address word. The outputs of this register are decoded by the decoding logic, and selection signals are generated to select the location in memory specified by the address. The content of S does not always uniquely determine the address of the memory word. The locations in memory, particularly fixed memory, beyond the capacity of register S are selected by the content of S in conjunction with the erasable and fixed bank registers.

Data is transferred between registers of the central processor or from the central processor to other portions of the system through the write amplifiers. There are 16 write amplifiers, each of which is associated with one bit position in each of the registers. Data is applied to the write amplifiers as a result of readout from a flip-flop register or from other functional areas. The data is merely ORed and becomes available on the write lines as outputs WL01-WL16. Inputs to the write amplifiers from other functional areas include the content of the erasable and fixed bank registers, inputs representing the addresses of the input counters in priority control, program interrupt addresses, control pulses from the sequence generator which are used during specific instructions, information from the input/output channels including the real time word, the start address, and the word from the CTS during test.

4-5.5.2 <u>Flip-Flop Register Operation Detailed Description</u>. A single bit position of flip-flop registers Q and Z is illustrated in figure 4-139. The description in the following paragraphs details operation of these bit positions, which are identical to all flip-flops in both registers. The concepts presented in this discussion are basic to all flip-flop registers in the central processor. Functional differences between the registers are described under the specific register headings.

Each of the flip-flop registers has a capacity of 16 bits. Four bit positions of each register are contained in each of four identical bit modules (A8-A11). For

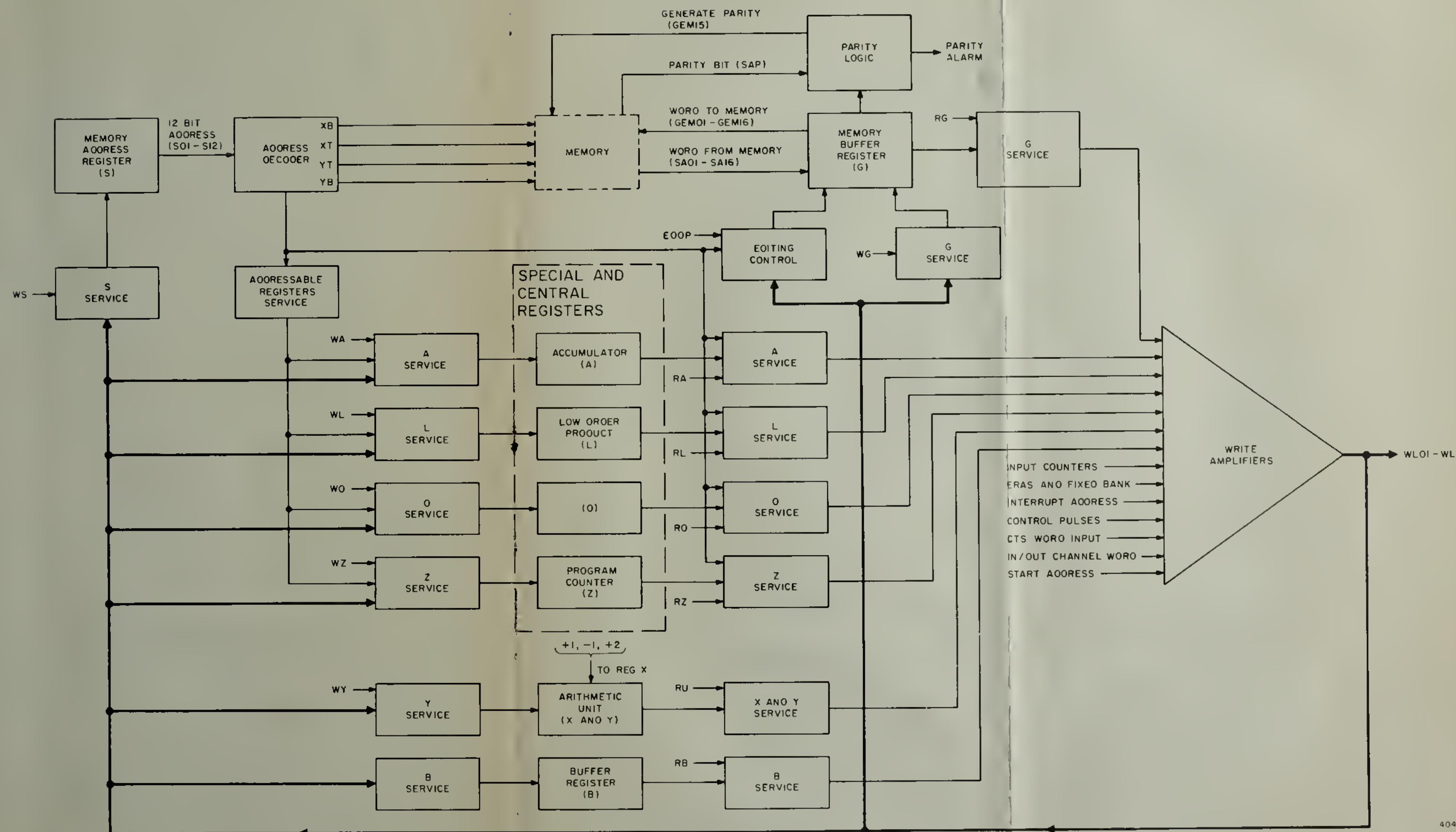

Figure 4-138. Central Processor Functional Diagram

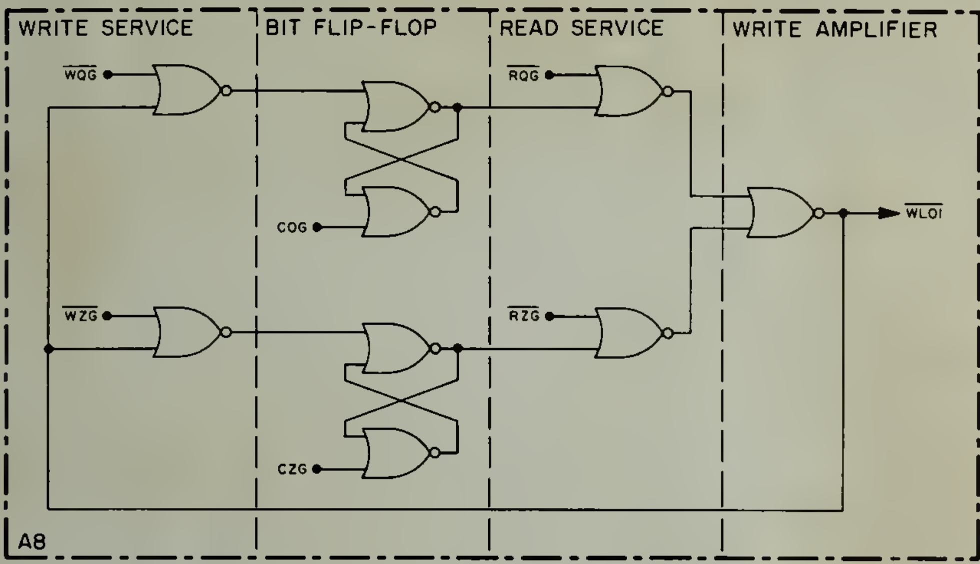

Figure 4-139. Flip-Flop Register, Single Bit Positions

example, module A8 contains bits 1 through 4 of all registers, module A9, bits 5 through 8, etc. Each bit position of the registers consists of a bit flip-flop and the write service and read service gates. The bit output is applied to an associated write amplifier. The entire register is cleared by a clear or reset pulse (CQG or CZG) applied directly to the reset input of each bit position. Information is written into the register from the write lines ($\overline{\text{WL01}}$) when the write signal ($\overline{\text{WQG}}$ or $\overline{\text{WZG}}$) enables the write service gate. The flip-flop is cleared and immediately written into. The read signal enables the read gate and causes the information stored in the flip-flop to be placed on the write lines. The write line outputs are labeled $\overline{\text{WL01}}$ through $\overline{\text{WL16}}$ corresponding to the bit positions of the registers. By enabling the read gates of register Z, and the write gates of register Q simultaneously, information is transferred between the two registers. This can be accomplished between any two registers in the central processor.

4-5.5.3 Register Service Gates. Information is transferred into and out of the flip-flop registers under control of write, clear, and read signals generated by associated write and read service gates for each register. Inputs to the service gates consist of write and read control pulses from the crosspoint matrix of the sequence generator and timing signals $\overline{\text{WT}}$, $\overline{\text{CT}}$, and $\overline{\text{RT}}$ (write time, clear time, and read time respectively) from the timer.

The write signals for each register are derived by gating a write control pulse and timing signal $\overline{\text{WT}}$. The clear pulse is derived as a function of the write signal and timing signal $\overline{\text{CT}}$. The read signal for each register is derived by gating a read control pulse and timing signal $\overline{\text{RT}}$. The write, clear, and read signals for register Z are illustrated in figure 4-140 and discussed in the following paragraphs.

Write control pulse $\overline{WZ}$ from the sequence generator is a 0.75 microsecond pulse and is illustrated as occurring at time 5 (T05) of a particular instruction. This control pulse coincident with timing signal $\overline{WT}$ results in 0.50 microsecond write signal $\overline{WQG}$ from the write service gates. The clear or reset pulse, CQG, is generated by gating the write signal $\overline{WQG}$ and timing $\overline{CT}$. This is a 0.25 microsecond positive transition and occurs during the first half of the enabling portion of the write signal as shown in figure 4-140. Thus, the flip-flop is cleared and the register immediately written into. The clear pulse occurs only when a write signal is generated; therefore, information written into the register is retained until the next write signal occurs.

The read control pulse $\overline{RZ}$, similar to the write control pulse, is 0.75 sec wide, and is shown in figure 4-140 as occurring at time 8 (T08). This signal from the sequence generator is gated with timing signal $\overline{RT}$ to produce read signal $\overline{RZG}$ from the read service gates. The read signal enables the read gates and causes information in the registers to be placed on the write lines. The read signal does not destroy the content of the register. Information is retained in each flip-flop and can actually be read out several times until the next write signal occurs. A detailed discussion of the write and read service for each register is included with the discussion on the flip-flop registers.

4-5.5.3.1 Addressable Registers Service. The four special and central registers (A, L, Q and Z) are addressable registers in that write, clear, and read signals can be generated as a function of an associated address supplied by the program. This is in addition to the write and read signals generated normally as described previously for all registers. These addresses are 0000 for register A, 0001 for register L, 0002 for register Q, and 0005 for register Z. The addresses in conjunction with timing signals $\overline{WT}$ and $\overline{RT}$ enable the service gates for write-in and readout.

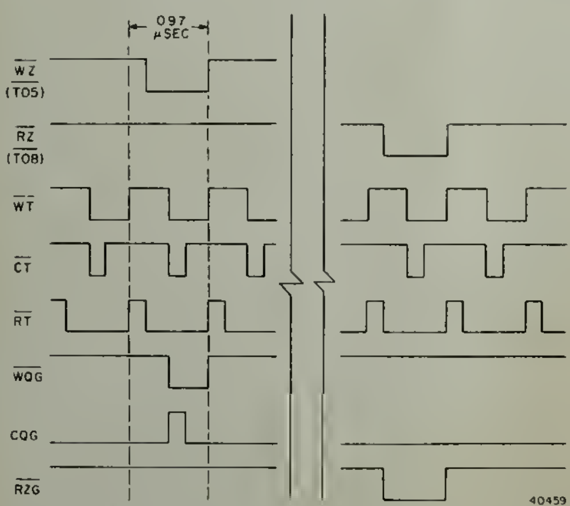

Figure 4-140. Write, Clear, and Read Timing

Write and read control signals are generated for the addressable registers by the logic illustrated in figure 4-141. Inputs $\overline{\text{WSC}}$ and $\overline{\text{RSC}}$, control pulses generated in the sequence generator, gate with timing signals $\overline{\text{WT}}$ and $\overline{\text{RT}}$ respectively to produce write signal $\overline{\text{WSCG}}$ and read signal $\overline{\text{RSCG}}$. These signals are applied to the service gates of each of the four registers along with the address supplied by the program. The register to be written into and readout of is determined by the address. Signal $\overline{\text{SCAD}}$ enables the gates if any one of octal addresses 0000 through 0007 is present. There is no access to memory at this time since signal SCAD is a logic ONE and inhibits erasable memory cycle timing. For all addresses above octal 0007, at least one of the inputs to gates 39345 and 39346 is a ONE and inhibits the addressable register service.

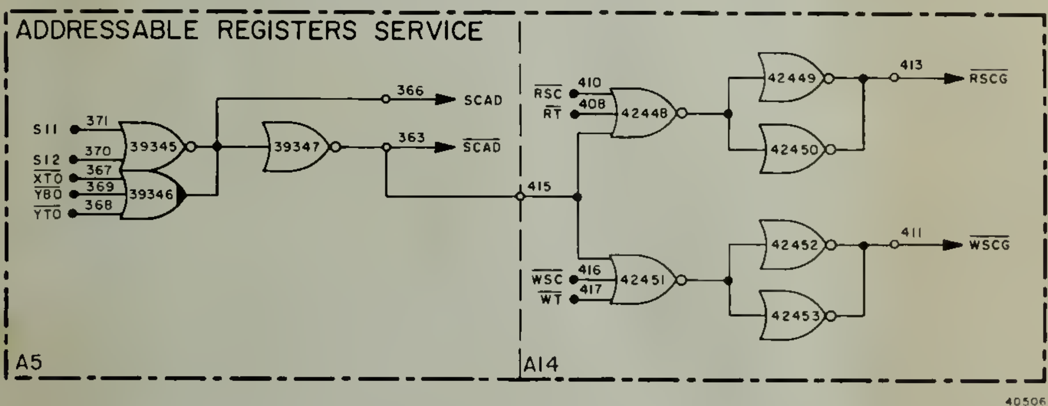

Figure 4-141. Addressable Registers Service

4-5.5.4 Register A. Register A (see figure 4-142), or accumulator, normally retains information between the execution of individual instructions. This is accomplished by write signal $\overline{\text{WAG}}$ from the write services (figure 4-143) which gates information on the write lines ($\overline{\text{WL01}}$ - $\overline{\text{WL16}}$) into register A. The write signal is generated as a function of control pulse $\overline{\text{WA}}$ from the sequence generator and timing signal $\overline{\text{WT}}$, or by octal address 00000 (indicated by $\overline{\text{XB0}}$) supplied by program and control pulse $\overline{\text{WSCG}}$. Either write condition causes the clear pulse CAG to be generated and clear the register prior to write-in. Write signal $\overline{\text{WALSG}}$ is generated to write into register A as a function of control pulse $\overline{\text{ZAP}}$. This latter control pulse is produced during multiply subinstructions MP1 and MP3 during which time the accumulator is used in conjunction with register L to form a double precision quantity accumulator. Write signal $\overline{\text{WALSG}}$ causes the write line inputs to be deposited into register A as indicated in table 4-LXXVI (the bit content of register L is also shown).

This manipulation of data accomplishes the required shifting during a multiply instruction.

4-5.5.5 Register L. Register L (see figure 4-142) functions during instruction MP (multiply) and DV (divide) and during the addition of double precision quantities. During instruction MP, register L holds the low order product; during instruction DV, the remainder.

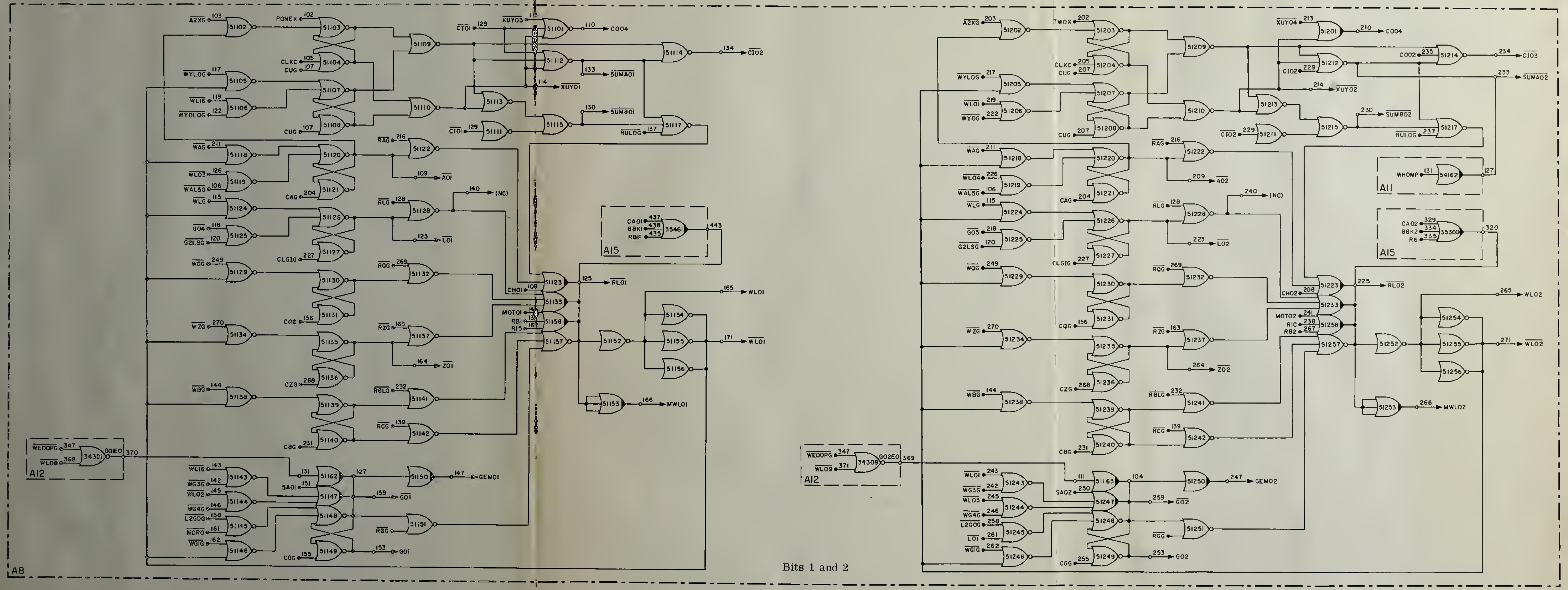

Figure 4-142. Flip-Flop Registers,
(Sheet 1 of 8)

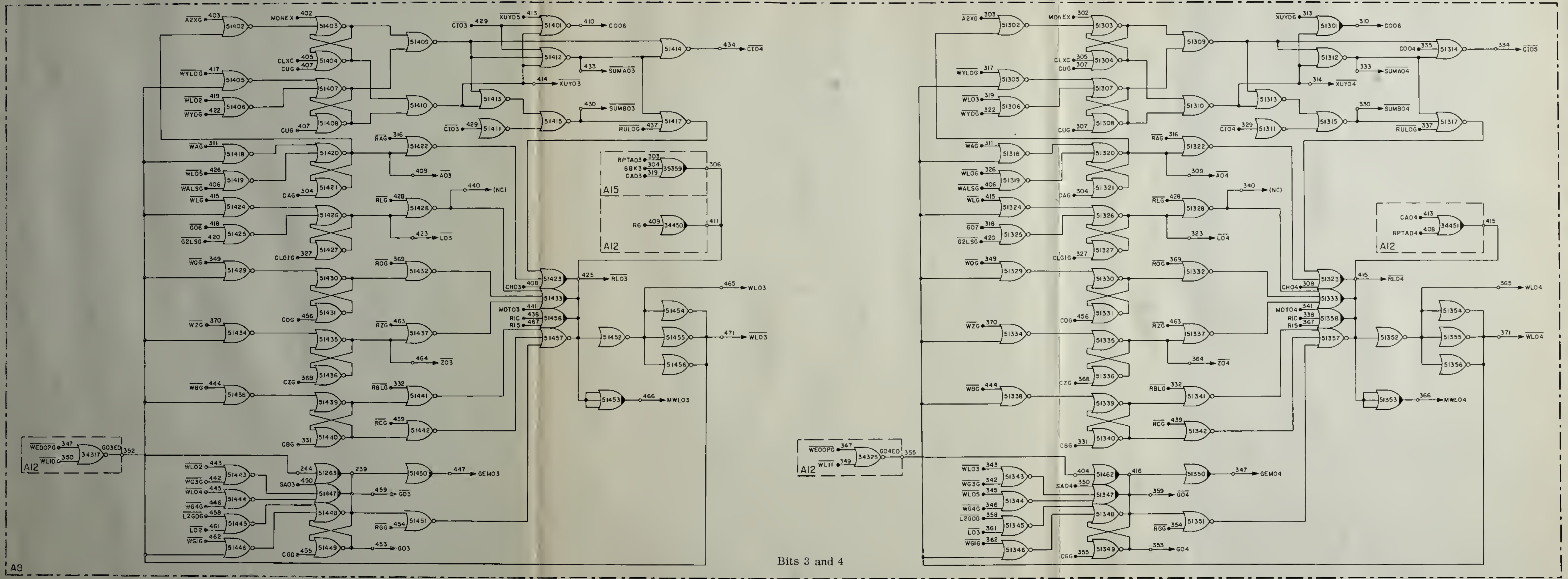

Figure 4-142. Flip-Flop Registers
(Sheet 2 of 8)

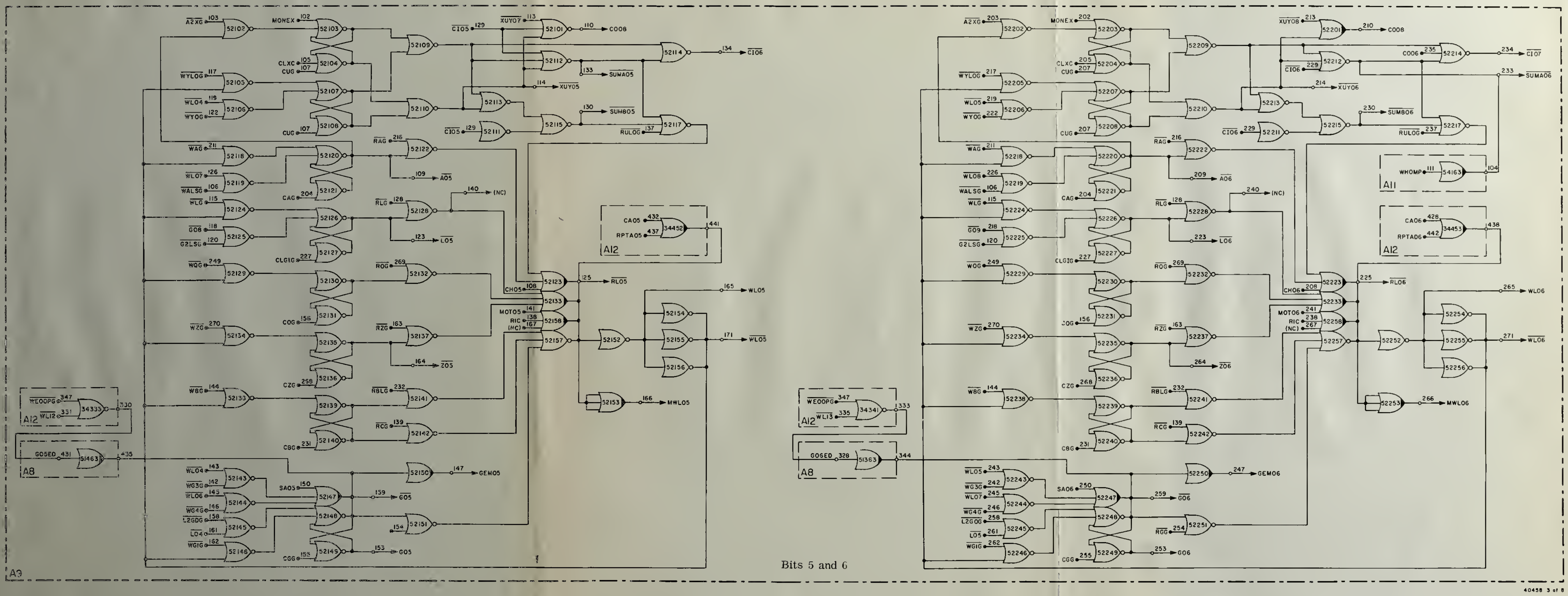

Figure 4-142. Flip-Flop Registers,
(Sheet 3 of 8)

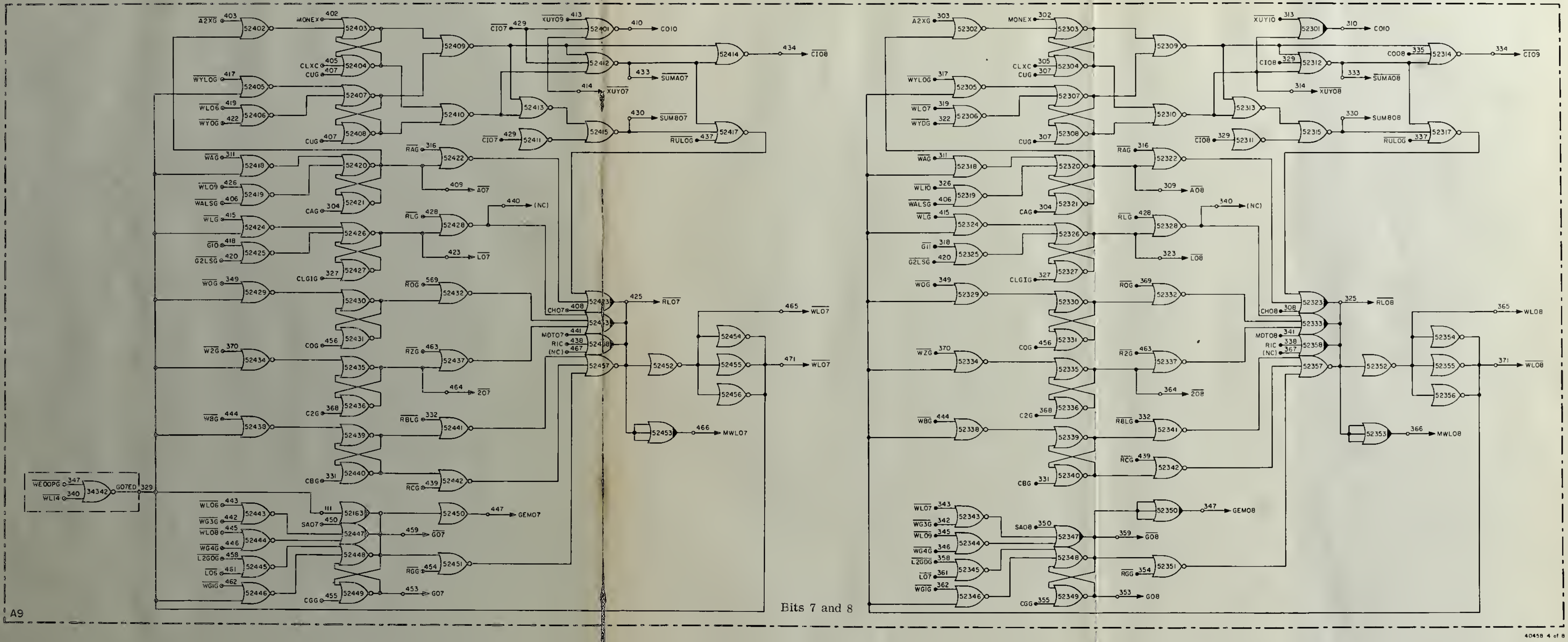

Figure 4-142. Flip-Flop Registers, (Sheet 4 of 8)

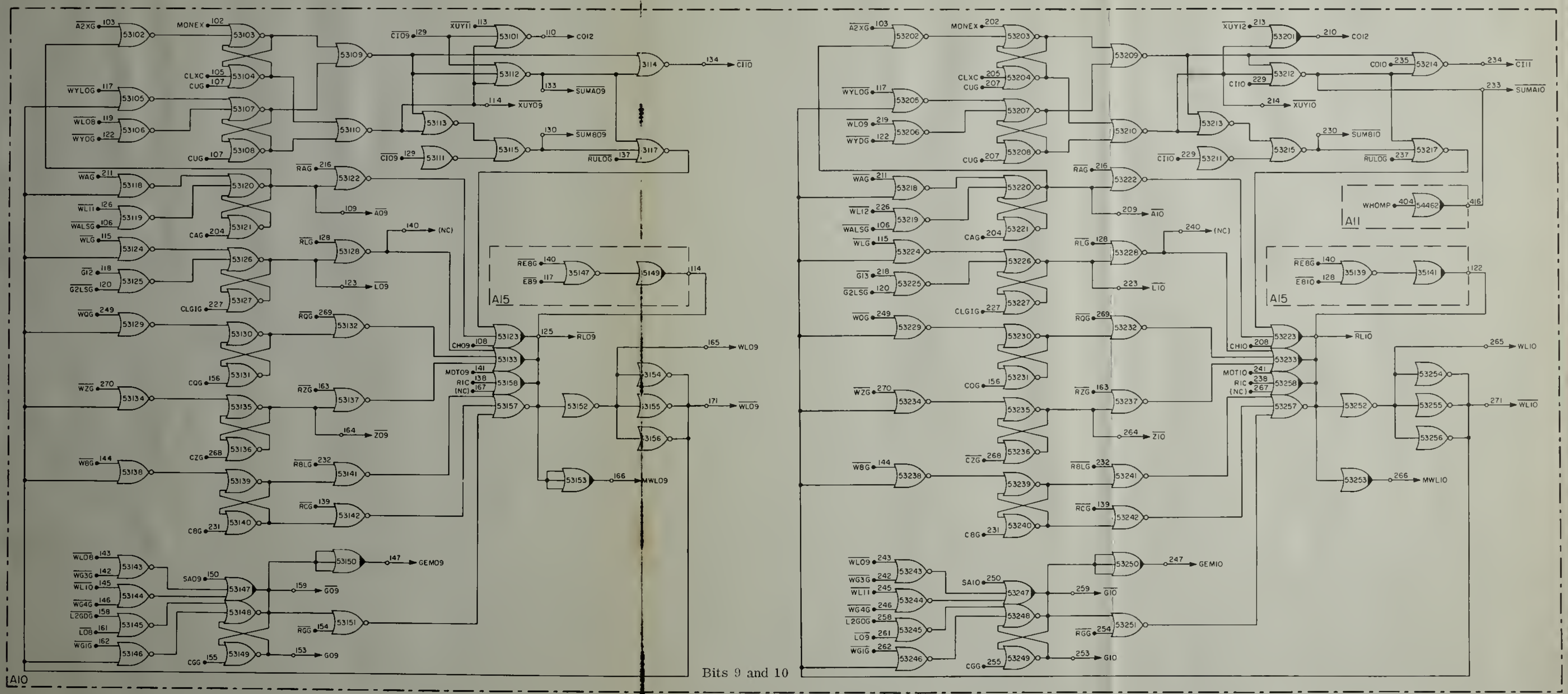

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Figure 4-142. Flip-Flop Registers, (Sheet 5 of 8)

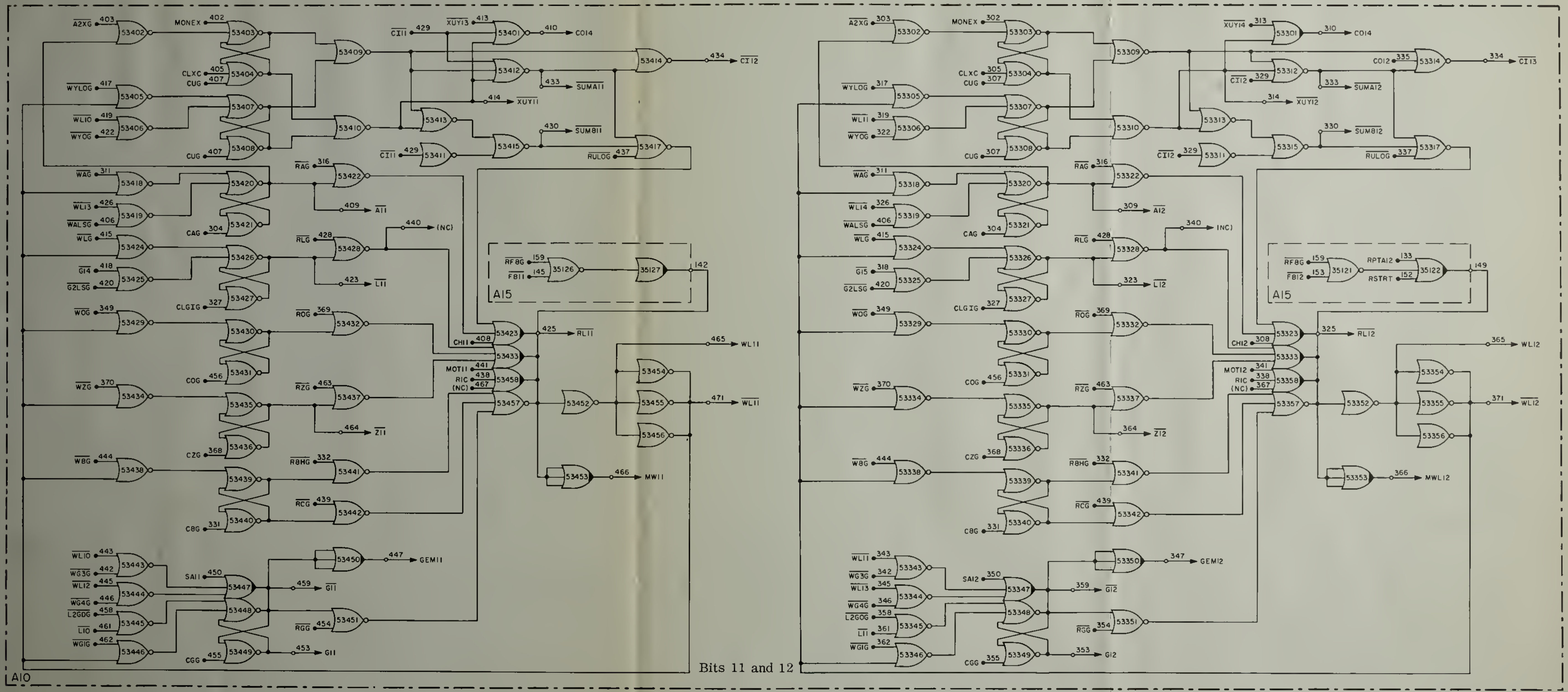

Figure 4-142. Flip-Flop Registers, (Sheet 6 of 8)

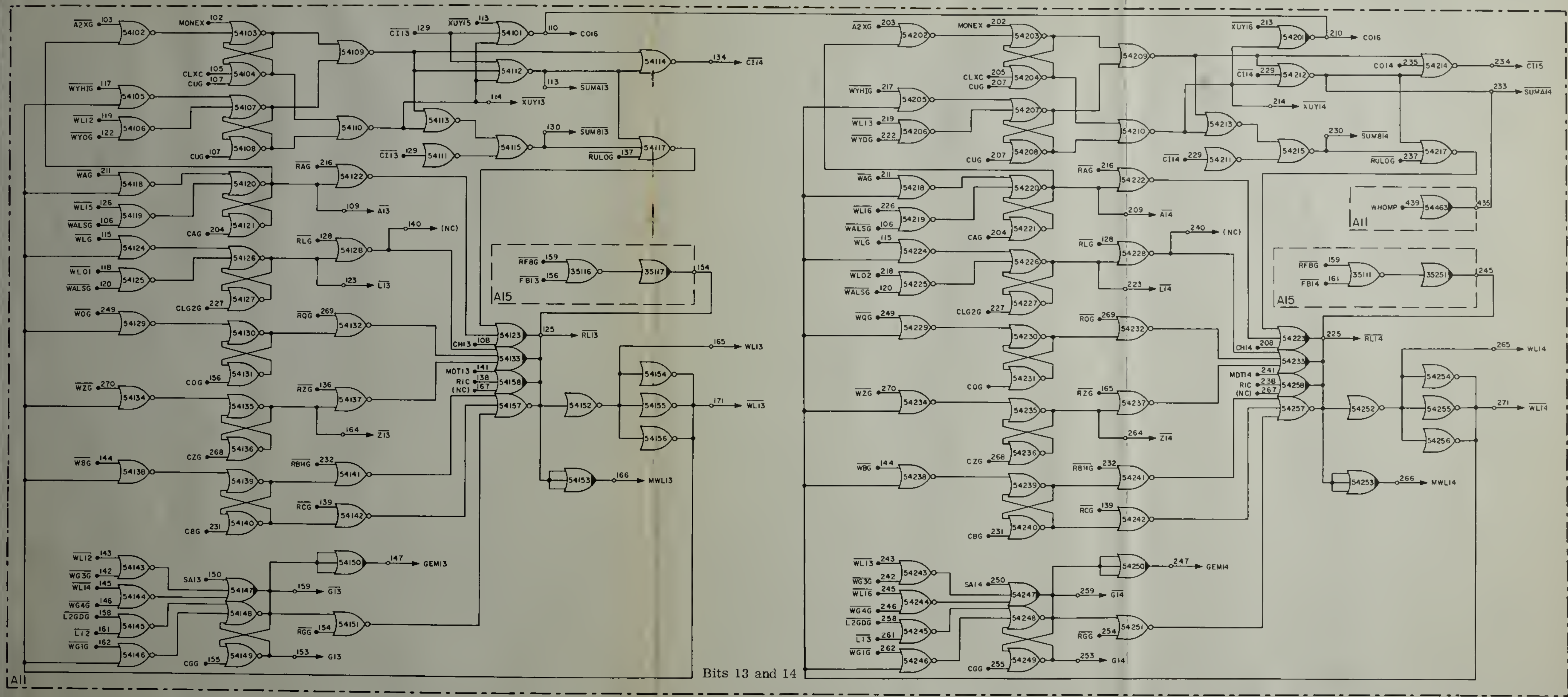

Figure 4-142. Flip-Flop Registers, (Sheet 7 of 8)

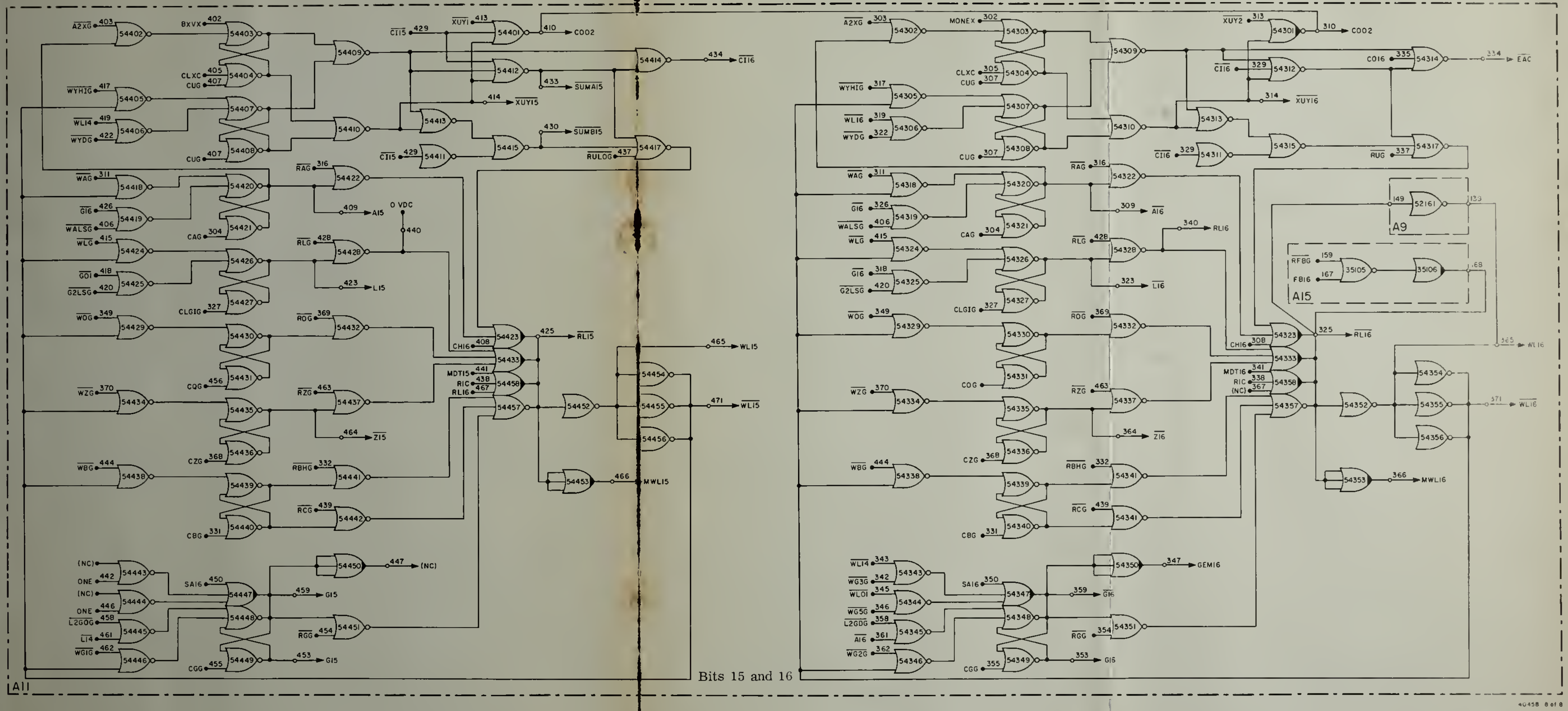

Figure 4-142. Flip-Flop Registers, (Sheet 8 of 8)

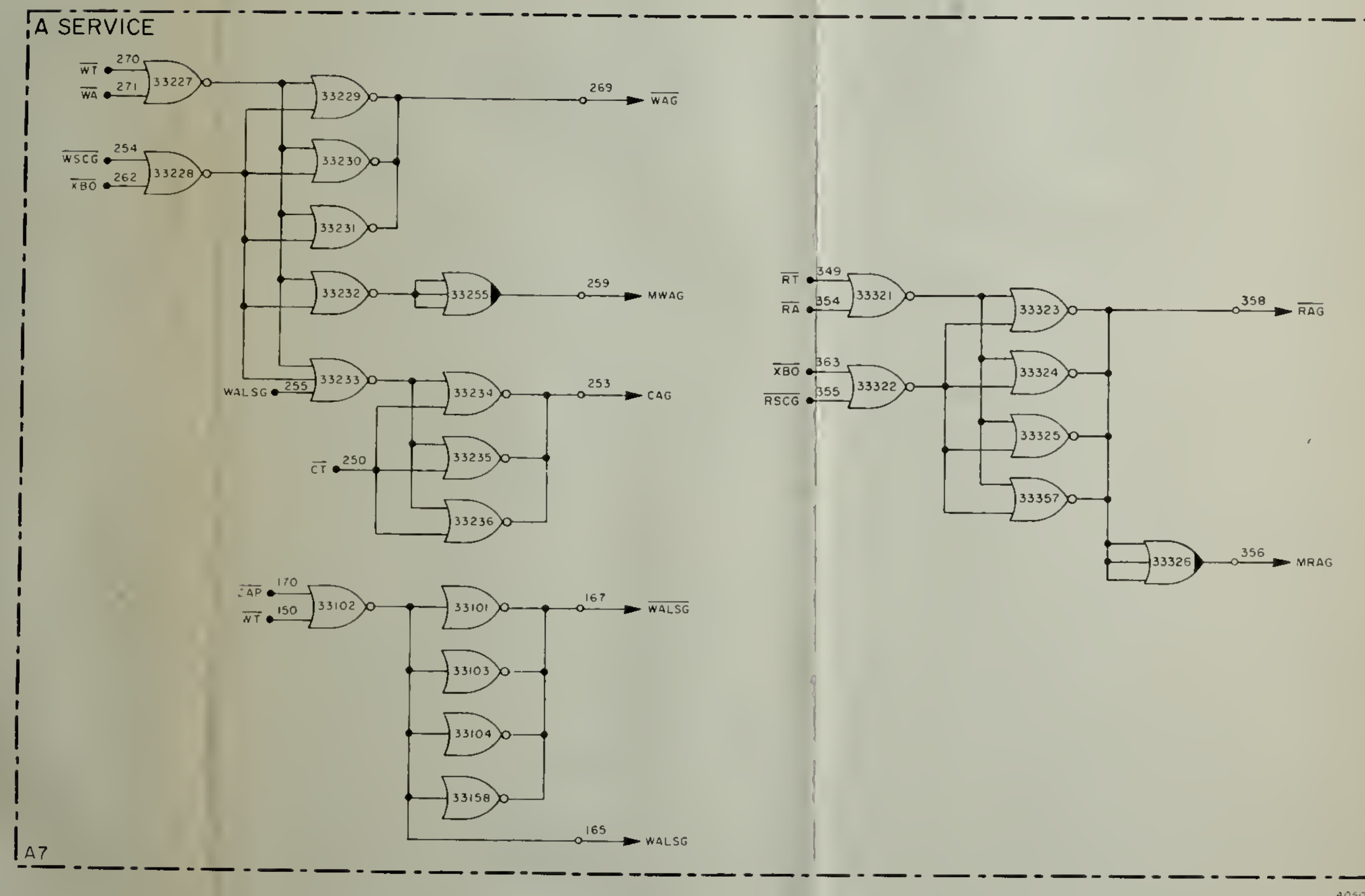

Figure 4-143. Register A Service

Table 4-LXXVI. Register A and L Write Line Inputs

A BIT															
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
G16	G16	WL16	WL15	WL14	WL13	WL12	WL11	WL10	WL09	WL08	WL07	WL06	WL05	WL04	WL03

L BIT															
16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
G16	G01	WL02	WL01	G15	G14	G13	G12	G11	G10	G09	G08	G07	G06	G05	G04

The L service gates (figure 4-144) generate the necessary write, clear and read signals. Write signal $\overline{WLG}$ is generated as a function of three inputs:

(1) Control pulse $\overline{WL}$ from the sequence generator.

(2) Special and central address 0001.

(3) Channel address 01.

Write control pulse $\overline{WL}$ is generated during most of the instructions for which register L is used. These include instructions DV, DAS (add double precision), and subinstruction MP0. Register L, similar to register A, is addressable. Under program control, octal address 0001 (indicated by $\overline{XB1}$ to the service gates) coincident with the addressable registers write control signal $\overline{WSCG}$ causes write signal $\overline{WLG}$ to be generated. Register L is also accessible with IN/OUT channel address 01. A channel instruction generates write control pulse $\overline{WCHG}$. This control pulse coincident with channel address 01 generates write signal $\overline{WLG}$.

A fourth condition for writing into register L is provided by write signal $\overline{G2LSG}$. This signal is generated during subinstructions MP1 and MP3 and occurs coincident with write signal $\overline{WALSG}$ for register A (both are generated as a function of control pulse $\overline{ZAP}$). The bit content of L as a result of write signal $\overline{G2LSG}$ is listed in table 4-LXXVI. Signal $\overline{G2LSG}$ allows writing into bit positions 1 through 12 and 15 and 16; signal $\overline{WALSG}$ allows writing into bit positions 13 and 14.

The clear signal for register L is generated as a function of the write-in conditions described above and control pulse $\overline{CT}$.

4-5.5.6 Register Q. Register Q (see figure 4-142) is used during instructions TC (transfer control) and QXCH (exchange). During a TC instruction, the return address is stored in Q in the event that a transfer to the original sequence of instructions takes place. During QXCH instruction, the quantity in Q is exchanged with a quantity in E memory.

The manipulation of data in register Q is determined by the write and read signals generated by the Q service gates (figure 4-145). These signals are produced in a manner similar to that described for the other registers. Control pulse $\overline{WQ}$ from the sequence generator is produced during instructions TC and QXCH, and causes write signal $\overline{WQG}$ to be generated. The write signal is also generated as a function of memory address 0002 (indicated by $\overline{XB2}$ to the service gates) coincident with the addressable registers write control signal $\overline{WSCG}$. The Q register is also accessible with IN/OUT channel address 02. The channel instruction write signal $\overline{WCHG}$ coincident with channel address 02 ($\overline{XTO}$. $\overline{XB2}$) causes write signal $\overline{WQG}$. Any one of the three write-in conditions described above causes the register clear pulse CQG to be generated. The read signal $\overline{RQG}$ is generated to read out the Q register as described for registers A and L.

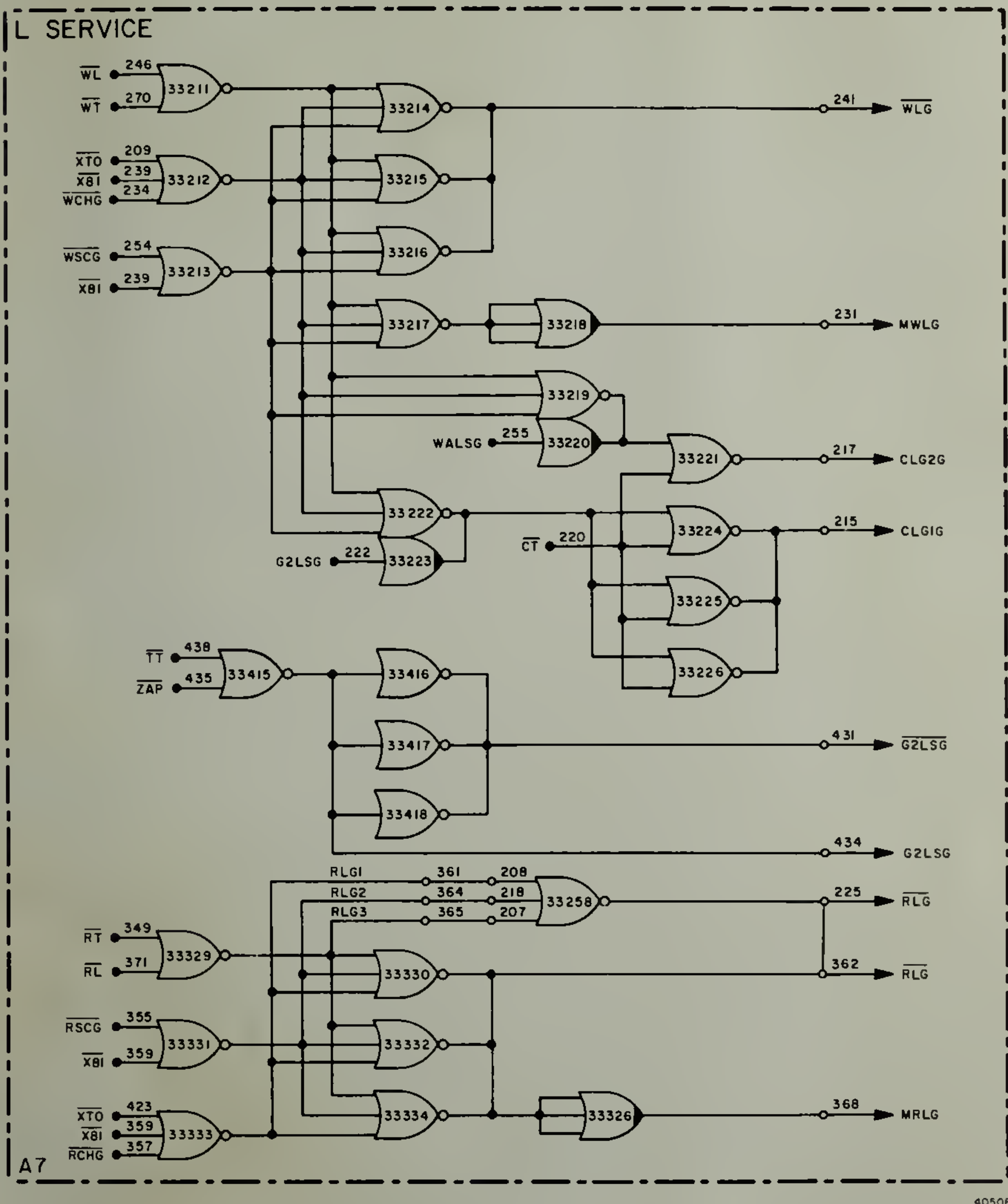

Figure 4-144. Register L Service

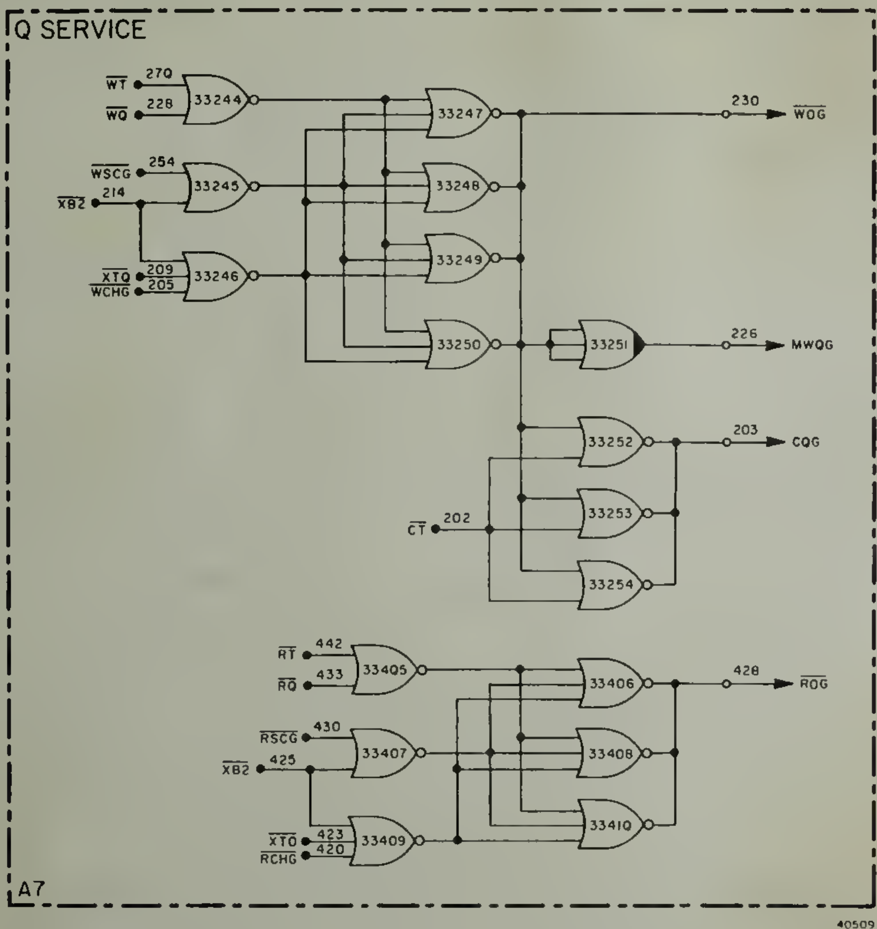

Figure 4-145. Register Q Service

4-5.5.7 Register Z. Register Z (see figure 4-142), also referred to as the program counter, stores the address of the instruction to be executed next. During the cxecution of an instruction, the content of register Z is incremented by one in the adder. The result (next address) is again stored in register Z. The write, clear, and read service (figure 4-146) generates the signals necessary to write into and read out of register Z. These are generated similar to those for registers A, Q, and L, with the exception that memory address 0005 ($\overline{\text{XB5}}$ to the service section) is used to write in and read out coincident with the addressable registers write and read control signals.

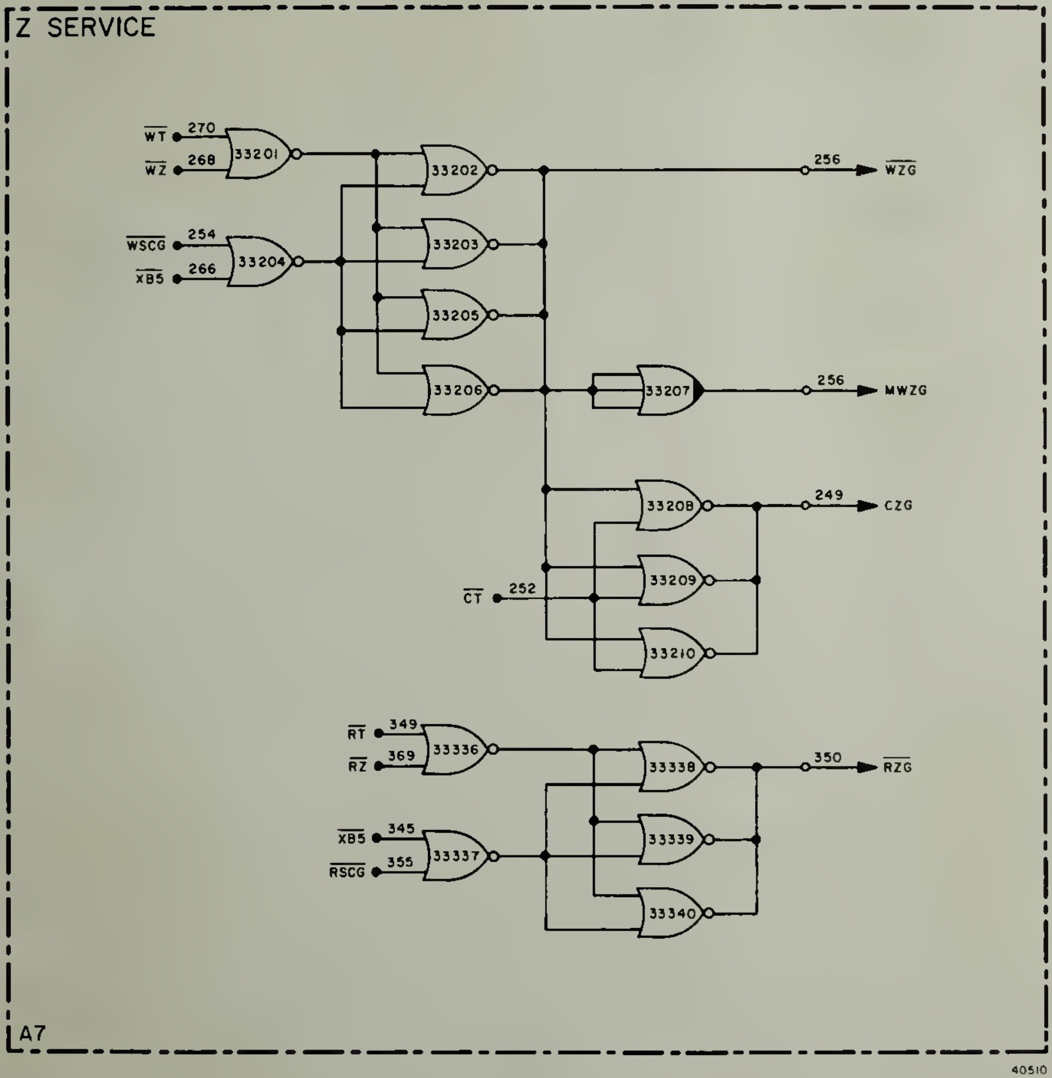

Figure 4-146. Register Z Service

Register Z write-in conditions for bit positions 15 and 16 also include the configuration illustrated in figure 4-147. During instruction DV1 (divide), a test for sign takes place (indicated by $\overline{BR1}$ to gate 39401). If the sign is negative, a ONE is inserted into bit position 16 of register Z at time 5 ($\overline{T05}$); at time 9, after a second test for sign, a ONE is inserted into bit position 15 of register Z if the sign is negative.

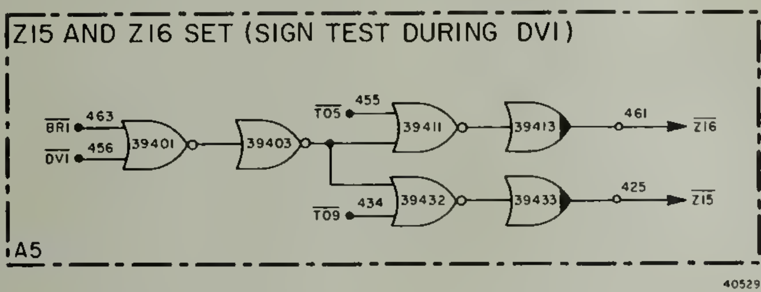

Figure 4-147. Z15 and Z16 Set (Sign Test During DV1)

4-5.5.8 Register B. Register B (see figure 4-142) is primarily a storage element. This register stores the order code and relevant address of the instruction to be executed next. This is not in conflict with register Z which stores the next address in the program.

The write, clear, and read signals for register B are generated by the service section (figure 4-148), in the same manner as described previously. This register is not addressable through program control. Readout of register B is accomplished normally by read control pulse $\overline{RB}$ from the sequence generator. This pulse causes read signals $\overline{RBHG}$ and $\overline{RBLG}$ to be generated. Signal $\overline{RBLG}$ reads out bit positions 1 through 10; signal $\overline{RBHG}$ reads out bit positions 11 through 16. Bit positions 1 through 10 only can be read out and placed on the write lines by $\overline{RBLG}$ which is generated as a function of signal RL10BB. This latter signal is generated during certain instructions to place the 10 low order bits of B on the write lines. Read signal $\overline{RCG}$ gates the complement of register B onto the write lines when required during certain instructions.

4-5.5.9 Register G. Register G (see figure 4-142) buffers all information coming from and going to erasable and fixed memory. This register also functions during certain instructions to shift or cycle information as required.

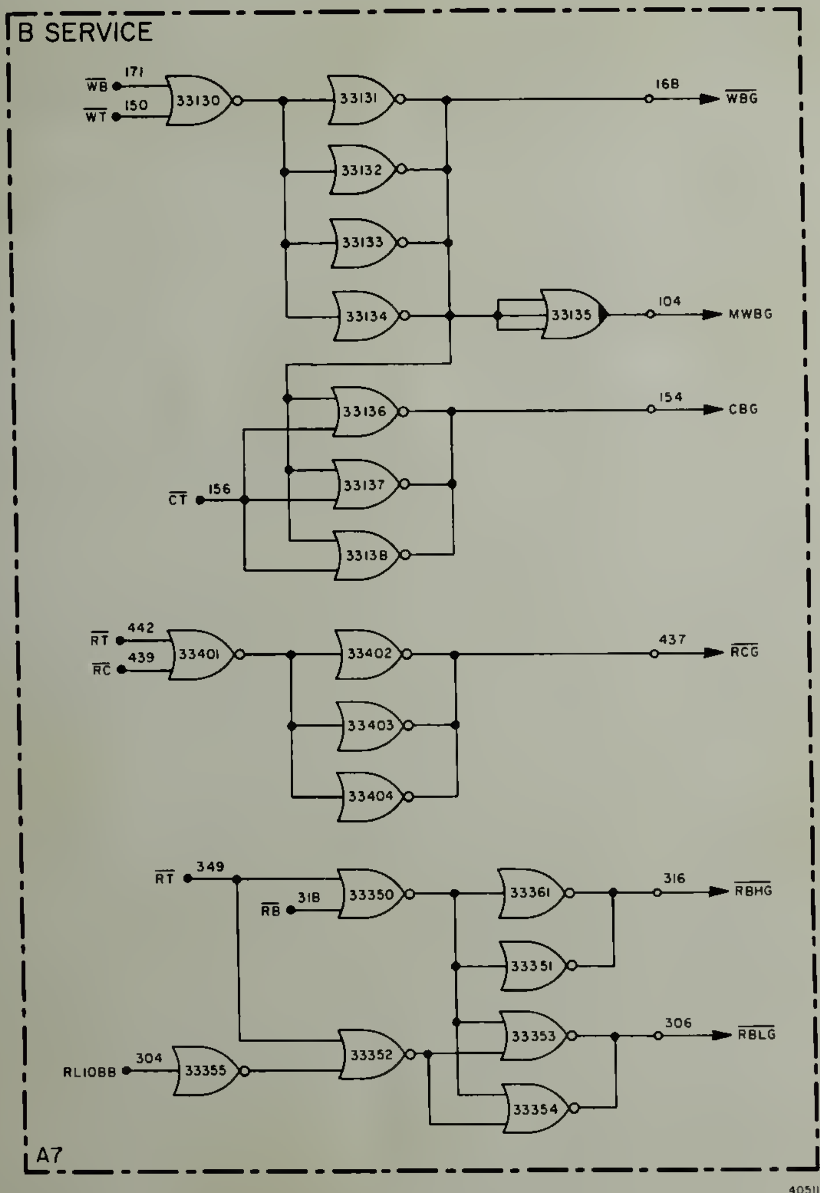

Figure 4-148. Register B Service

Data from fixed or erasable memory is written into register G from sense amplifier outputs SA01 through SA14 and SA16, which are wired directly into the corresponding bit positions of register G. Sense amplifier output SA16 which is the sign bit, is wired into both bit positions 15 and 16 of G. This results in the same bit value in these two bit positions when a quantity is entered into the central processor from memory as described previously under word formats.

There is no manipulation of the parity bit within the central processor. Consequently, register G never sees this bit during readout or write-in to memory. The parity logic controls all manipulations of the parity bit.

Write service for register G (figure 4-149), consists of six write signals, $\overline{WG1G}$ through $\overline{WG5G}$ and $\overline{WEDOPG}$. For all addresses except octal 0020 through 0023, write signals $\overline{WG1G}$ and $\overline{WG2G}$ are generated and information is gated from the write lines into register G. Write signal $\overline{WG1G}$ gates bit positions 1 through 15; write signal $\overline{WG2G}$ gates bit position 16. These two signals are produced by write control pulse $\overline{WG}$ from the sequence generator (which appears as $\overline{WGA}$ in G service) coincident with timing pulse $\overline{WT}$ into gate 33140 of figure 4-148. This results in WGNORM which causes write signals $\overline{WG1G}$ and $\overline{WG2G}$. Signal GINH from the editing control logic inhibits write signal $\overline{WG1G}$ during shift and cycle operations. Bit position 15 is not used during any shifting and cycling operations.

Octal addresses 0020 through 0023 are produced under program control to perform shift and cycle operations. The decoded signals representing these addresses are applied to the editing control logic (figure 4-150) which generates the signals necessary to manipulate data into register G. Signal OCTAD2 is inverted by gate 34343 and enables the input gates of editing control for octal addresses 0020 through 0027. The cycle and shift control signals are generated at time 2 ($\overline{T02}$) coincident with the particular address.

Address 0020 causes a word to be cycled right when entered into register G. The decoded signals representing this address ($\overline{OCTAD2} \cdot \overline{XB0}$) set the cycle right control flip-flop in editing control at time 2. The flip-flop output ($\overline{CYR}$) enables the write gates in the service section, and, coincident with write control pulse $\overline{WGA}$, causes write signals $\overline{WG4G}$ and $\overline{WG5G}$ to be produced. Data is cycled right as shown in figure 4-151. The programmer would consider this transformation as follows:

CYR	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit Position
0020	01	15	14	13	12	11	10	09	08	07	06	05	04	03	02	G Register

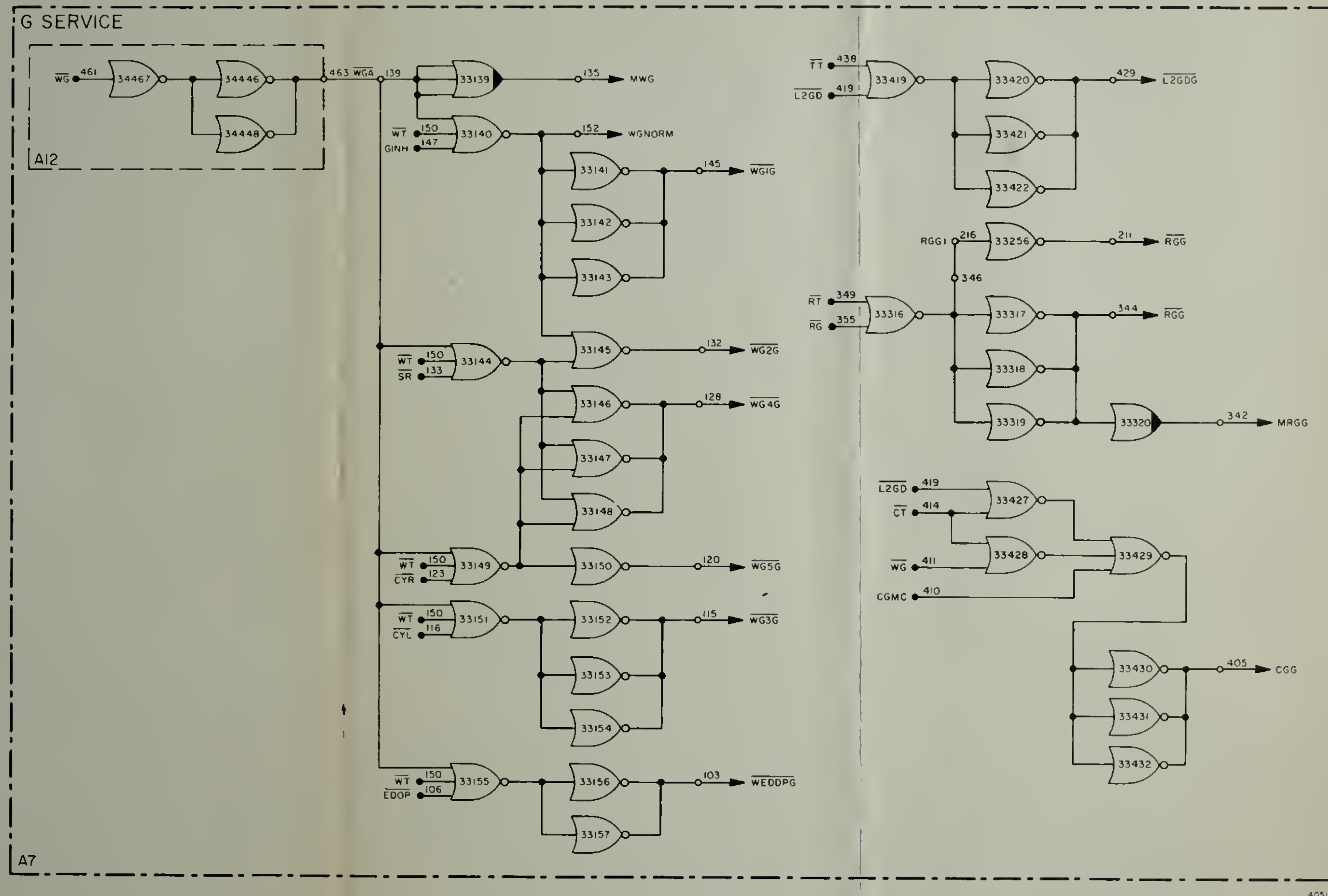

Figure 4-149. Register G Service

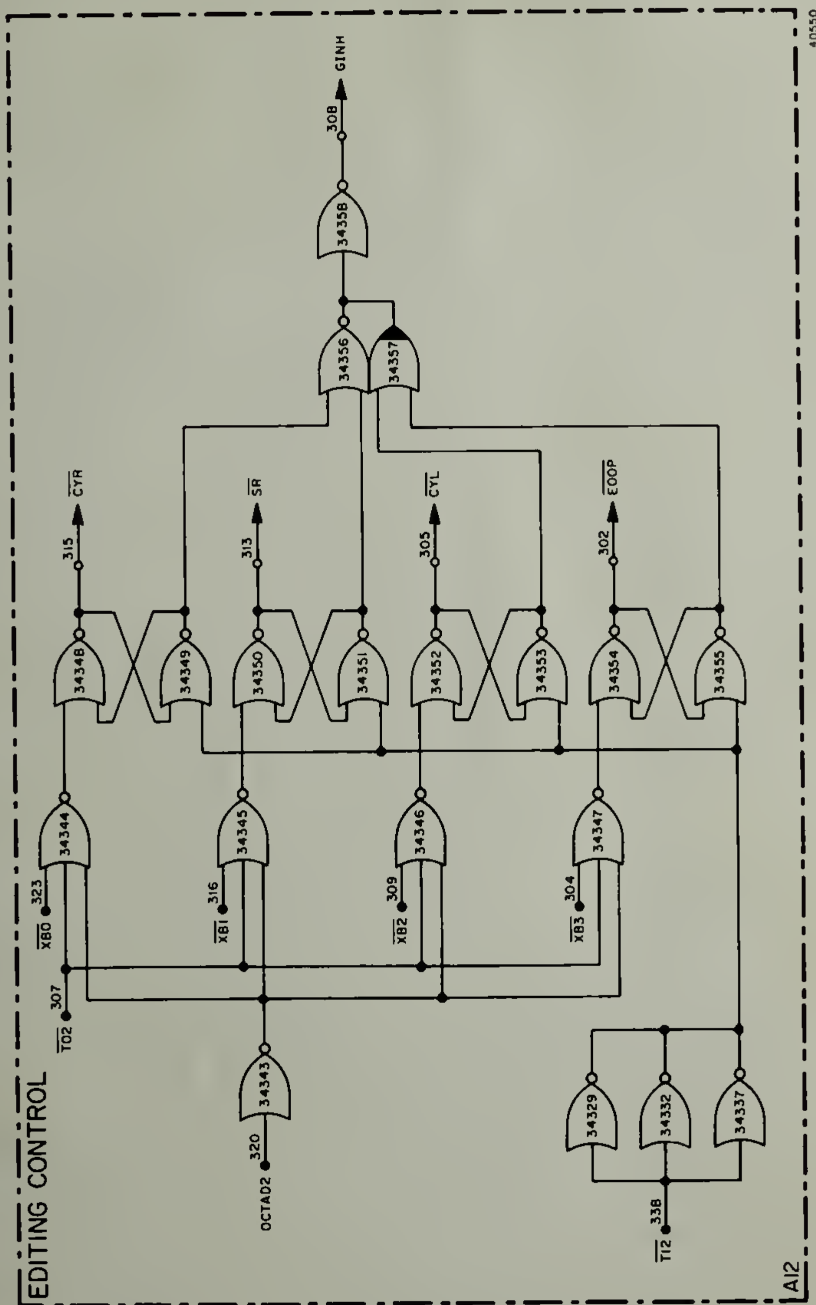

Figure 4-150. Editing Control

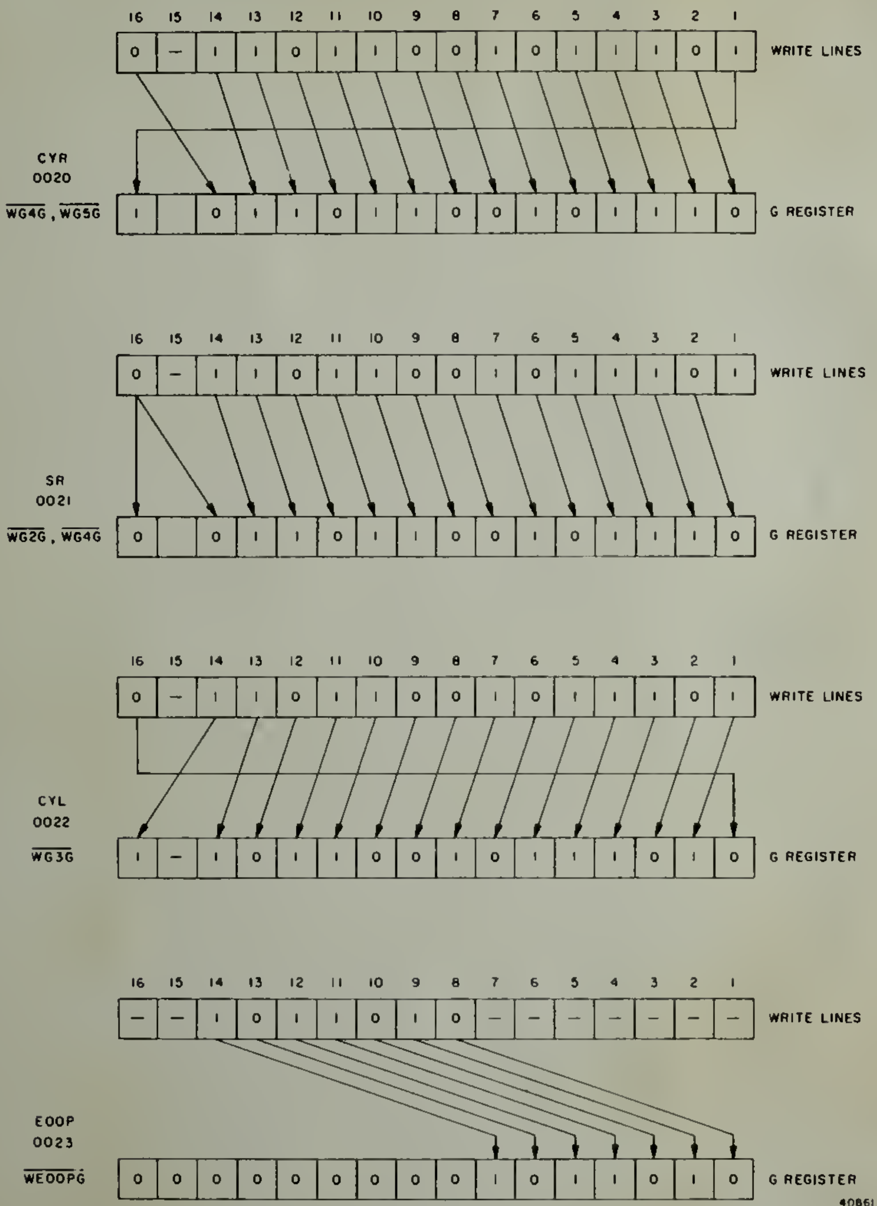

Figure 4-151. Editing Transformations

Address 0021 ($\overline{OCTAD2} \cdot \overline{XB1}$) sets the shift right control flip-flop. The flip-flop output ($\overline{SR}$) enables the write control pulse $\overline{WGA}$, and causes write signals $\overline{WG2G}$ and $\overline{WG4G}$ to be produced. Bit 16 from the write lines is entered into bit positions 16 and 14 of register G, and all other bits are shifted one position to the right. No action occurs with bit 1 from the write lines - this bit is effectively shifted off the end. The programmer would consider this transformation as follows:

SR	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit Position
0021	15	15	14	13	12	11	10	09	08	07	06	05	04	03	02	G Register

Address 0022 ($\overline{OCTAD2} \cdot \overline{XB2}$) sets the cycle left control flip-flop. The flip-flop output ($\overline{CYL}$) enables the write gates, and, coincident with write control pulse $\overline{WGA}$, causes write signal $\overline{WG3G}$ to be produced for a cycle left operation. As shown in figure 4-151, bit 16 from the write lines is written into bit position 1 of G, bit 2 is written into bit position 3, etc. The programmer would consider this transformation as follows:

CYL	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit Position
0022	14	13	12	11	10	09	08	07	06	05	04	03	02	01	15	G Register

The last editing transformation involves bits 8 through 14 from the write lines. Address 0023 sets the edit operation flip-flop ($\overline{EDOP}$) in the editing control logic. The flip-flop output enables the associated write gates in the service section, and causes write signal $\overline{WEDOPG}$ to be produced. This signal writes bits 8 through 14 from the write lines into bit positions 1 through 7 of register G as illustrated in figure 4-151. The programmer would consider this transformation as follows:

EDOP	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit Position
0023	--	--	--	--	--	--	--	--	14	13	12	11	10	09	08	G Register

During divide and multiply instructions, the G register is used in the manipulation of data in the central processor. Write-in is accomplished by write signal $\overline{L2GDG}$ which is generated only during these instructions. The signal is generated as a function of

write control pulse $\overline{L2GD}$ from the sequence generator, and timing pulse $\overline{TT}$ from the timer. Signal $\overline{TT}$ is identical to the write time signal $\overline{WT}$. The content of register G after write-in by $\overline{L2GDG}$ is as follows:

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
MCRO	L01	L02	L03	L04	L05	L06	L07	L08	L09	L10	L11	L12	L13	L14	L16

Bit position 16 contains bit 16 from the accumulator, positions 15 through 2 contain L bits 14 through 1 respectively, and the data in bit position 1 is a function of control pulse $\overline{MCRO}$. This latter control pulse is generated in the sequence generator as a function of the content of register L during a multiply instruction and enters a ONE into bit position 1 of the G register. The clear signal for register G (CGG) is generated as a function of write signals $\overline{WG}$ and $\overline{L2GD}$ coincident with timing pulse $\overline{CT}$. Register G is also cleared by signal CGMC. This signal is generated as a function of the strobe signals for erasable and fixed memory. When the sense amplifiers are strobed (STBE or STBF), signal CGMC is generated and clears register G.

The read signal ($\overline{RGG}$) is generated as a function of read control pulse $\overline{RG}$ and timing signal $\overline{RT}$.

4-5.5.10 Arithmetic Unit (Registers X and Y). The arithmetic unit (see figure 4-142) is a 16 bit parallel adder with end-around carry and is the basic arithmetic unit of the LGC. The adder processes two numbers at a time; one number is contained in register Y, and a quantity is entered into X by control pulse action dependent on the instruction being executed. The output gating complex senses for the carry and provides outputs from each bit position to the write lines.

Registers X and Y are functionally similar to the other flip-flop registers. However, the write service is more complex for register Y than for the other flip-flop registers. Register X has only one write signal ($\overline{A2XG}$), and this is constrained to register X being used in conjunction with register A during certain instructions.

Register Y is written into from the write lines; register X is not. The quantity entered into X is by control pulse action or by write signal $\overline{A2XG}$ as indicated above. The clear pulse (CUG) is generated as a function of the Y register write signals and clears both X and Y simultaneously.

The service gates for registers X and Y are illustrated in figure 4-152. Data from the write lines is written into the corresponding bit positions of register Y by write signals $\overline{\text{WYLOG}}$ and $\overline{\text{WYHIG}}$. Both of these signals are generated as a function of write control pulse $\overline{\text{WY}}$ and timing pulse $\overline{\text{WT}}$. Write signal $\overline{\text{WYLOG}}$ writes into bit positions 1 through 12; write signal $\overline{\text{WYHIG}}$ writes into bit positions 13 through 16. Signal $\overline{\text{WYLOG}}$ is also generated as a function of control pulse $\overline{\text{WY12}}$ from the sequence generator. This control pulse occurs during the execution of specific instructions to write into positions 1 through 12 of register Y. (Refer to the sequence generator which indicates the conditions for generating $\overline{\text{WY12}}$). In this case, positions 13 through 16 would not be written into and as a result of the clear pulse action would contain ZERO's.

Write signals $\overline{\text{WYDG}}$ and $\overline{\text{WYDLOG}}$ are generated during the multiply and divide instructions, and counter instructions SHINC and SHANC. There is some additional manipulation with bit position 1 of Y as a result of $\overline{\text{WYDLOG}}$. Write control pulse $\overline{\text{WYD}}$ is generated in the sequence generator and coincident with timing pulse $\overline{\text{WT}}$ generates write signals $\overline{\text{WYDG}}$ and $\overline{\text{WYDLOG}}$. The bit content of Y as a result of this write-in condition is as follows:

BIT	16	15	14	13	12	11	10	9
	$\overline{\text{WL16}}$	$\overline{\text{WL14}}$	$\overline{\text{WL13}}$	$\overline{\text{WL12}}$	$\overline{\text{WL11}}$	$\overline{\text{WL10}}$	$\overline{\text{WL09}}$	$\overline{\text{WL08}}$
BIT	8	7	6	5	4	3	2	1
	$\overline{\text{WL07}}$	$\overline{\text{WL06}}$	$\overline{\text{WL05}}$	$\overline{\text{WL04}}$	$\overline{\text{WL03}}$	$\overline{\text{WL02}}$	$\overline{\text{WL01}}$	$\overline{\text{WL16}}$

Bit 16 from the write lines is entered into positions 16 and 1 of Y; positions 15 through 2 contain write line inputs 14 through 1, respectively. Write-in to bit position 1 by $\overline{\text{WYD}}$ is inhibited by several functions. Interflow from the register A bit 1 is inhibited during a multiply instruction if bit 15 of register L contains a ONE. This condition is sensed by gate 33125 in the service section. Also, during multiply, end-around carry is inhibited. This condition is satisfied by signal NEAC (no end-around carry) to gate 33124. Lastly, during counter instruction SHINC (shift), write-in to bit position 1 is inhibited by counter command SHINC.

The write signal $\overline{\text{A2XG}}$ is generated to write into register X mostly during extracode instructions (the one exception is basic instruction AD-add). This signal copies the content of register A into the corresponding bit positions of register Y. This is illustrated in figure 4-142. The flip-flop outputs of A are wired directly to the only write gate inputs to register X, and are gated by signal $\overline{\text{A2XG}}$.

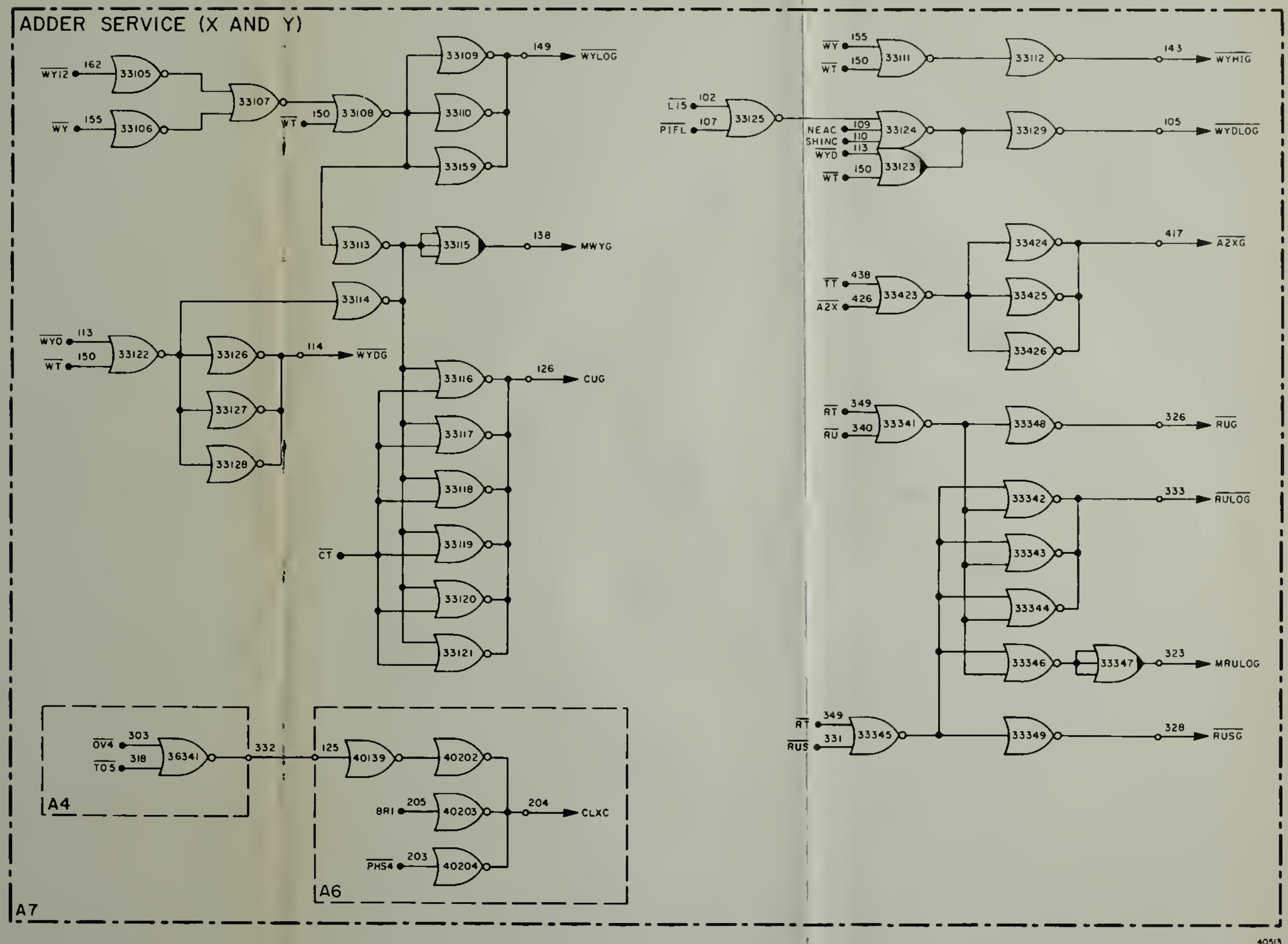

Figure 4-152. Adder Service (Registers X and Y)

Since the arithmetic unit processes two numbers, one number is obviously entered into Y from the write lines. Another quantity, dependent on the instruction being executed, is entered into register X. This is accomplished by control pulses PONEX, MONEX, TWOX, and BXVX. These control pulses enter the quantities +1, -1, +2 and 40000 (octal) respectively. The quantity +0 is effectively entered into X by clear signal CLXC. This signal occurs during a divide instruction as a result of a branching condition.

Two read signals are generated to read out the adder. Signal $\overline{\text{RULOG}}$ reads out positions 1 through 15; signal $\overline{\text{RUG}}$ reads out position 16 only. The two signals are generated simultaneously as a function of read control pulse $\overline{\text{RU}}$ coincident with timing signal $\overline{\text{RT}}$. Only bit positions 1 through 15 are read out by read signal $\overline{\text{RULOG}}$ which is generated as a function of control pulse $\overline{\text{RUS}}$. This control pulse is generated during extracode instruction MSU (modular subtract) and counter instructions PCDU, MCDU and SHIFT.

The carry gate output from each bit position ($\overline{\text{CI02}}$-$\overline{\text{CI15}}$) is applied to the next high order bit position ($\overline{\text{CI02}}$ from bit position 1 to bit position 2, etc). The end-around carry from bit position 16 ($\overline{\text{EAC}}$) is applied to bit position 1 through the carry logic (figure 4-153). End-around carry is inhibited during a multiply instruction. At time 10 of subinstruction MP0, FF40426-40427 is set and signal NEAC (no end-around carry) inhibits the carry-in gate. The gate is again enabled at time 6 of subinstruction MP3 which occurs at the end of the multiply instruction. A logic ONE is forced into bit position 1 during certain instructions by the carry-in flip-flop (FF33458-33459). Control pulse CI from the sequence generator sets this flip-flop, the output of which is applied as an enabling level to the carry-in gate of bit position 1. Clear signal CUG resets the flip-flop.

The quantities entered into the arithmetic unit during normal computations contain the sign in both positions 15 and 16. If overflow or underflow occurs, bit position 15 will contain a value bit which is opposite to the correct sign bit. A ONE in bit position 15 indicates overflow when both operands are positive; a ZERO in bit position 15 indicates underflow when both operands are negative. The correct sign of the sum is always contained in bit position 16.

4-5.5.11 Write Amplifiers. The write amplifiers consist of an extended NOR input configuration, the output of which is applied through an output driver. One write amplifier configuration is associated with each bit position of the flip-flop registers as shown in figure 4-142. Outputs WL01 through WL16 and their complements are available and are designated as the write lines. The write amplifiers function logically as an OR gate. If any one input is a logic ONE, output WL-- is a logic ONE, and the complement output $\overline{\text{WL--}}$ is a logic ZERO. The latter output is used extensively as an enabling level to transfer information from one register to another, and for other gating functions throughout the LGC.

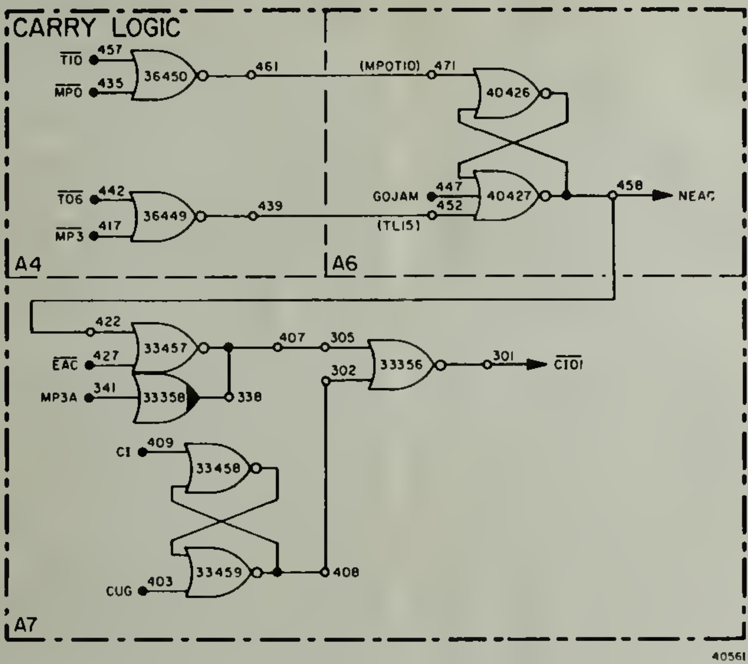

Figure 4-153. Carry Logic

The majority of inputs to the write amplifiers are from the flip-flop registers. The output from each bit position of the registers is wired directly to an associated write amplifier input. The 16 bit output of any one register involves the 16 write amplifiers contained in logic modules A8 through A11.

The inputs to the write amplifiers, excluding the flip-flop register inputs, are indicated in table 4-LXXVII and are described in the following paragraphs.

Inputs CAD1 through CAD6 are from the counter address generator in priority control, and determine the address of the counter in erasable memory which is to be updated. Since these inputs are applied to the six low-order bit positions, counters at locations up to 0077 could be addressed. However, the arrangement of counters in erasable memory at present involves addresses 0024 through 0060. A specific counter address is determined by the correct combination of inputs CAD1 through CAD6. This is illustrated as follows for the address of the time 6 (T6) counter - address 0031. For this address, inputs CAD5, CAD4, and CAD1 are logic ONE's; the remaining inputs are logic ZERO's. Inputs to write amplifiers 7 through 15 are not enabled; therefore, the full address is 00031 (octal).

Table 4-LXXVII. Write Amplifiers External Inputs

WL16	WL15	WL14	WL13	WL12	WL11	WL10	WL09	WL08	WL07	WL06	WL05	WL04	WL03	WL02	WL01
----	----	----	----	----	----	----	----	----	----	CAD6	CAD5	CAD4	CAD3	CAD2	CAD1
----	----	----	----	RPTAD12	----	----	----	----	----	RPTAD6	RPTAD5	RPTAD4	RPTAD3	----	----
----	----	----	----	----	----	----	----	----	----	----	----	----	BBK3	BBK2	BBK1
----	----	----	----	----	----	EB10	EB09	----	----	----	----	----	----	----	----
FB16	----	FB14	FB13	FB12	FB11	----	----	----	----	----	----	----	----	----	----
----	----	----	----	----	----	----	----	----	----	----	----	----	----	----	RB1F
----	----	----	----	----	----	----	----	----	----	----	----	----	R6	R6	----
----	----	----	----	----	----	----	----	----	----	----	----	R15	R15	----	R15
R1C	R1C	R1C	R1C	R1C	R1C	R1C	R1C	R1C	R1C	R1C	R1C	R1C	R1C	R1C	----
----	----	----	----	----	----	----	----	----	----	----	----	----	----	RB2	RB1
----	----	----	----	RSTRT	----	----	----	----	----	----	----	----	----	----	----
----	RL16	----	----	----	----	----	----	----	----	----	----	----	----	----	----
CH16	CH16	CH14	CH13	CH12	CH11	CH10	CH09	CH08	CH07	CH06	CH05	CH04	CH03	CH02	CH01
MDT16	MDT15	MDT14	MDT13	MDT12	MDT11	MDT10	MDT09	MDT08	MDT07	MDT06	MDT05	MDT04	MDT03	MDT02	MDT01

WRITE LINE	15 14 13	12 11 10	9 8 7	6 5 4	3 2 1
	0 0 0	0 0 0	0 0 0	0 1 1	0 0 1
	0	0	0	3	1

Inputs RPTAD3, 4, 5, 6, and RPTAD12 are placed on the write lines from the interrupt address generator in priority control. These inputs are used to determine one of addresses 4004, 4010, 4014, 4020, 4024, 4034, 4040, 4044, 4050, which are respectively the locations in fixed memory for the first instruction of the T6RUPT, T5RUPT, T3RUPT, T4RUPT, KEYRUPT, UPRUPT, DOWNRUPT, RADAR RUPT, and HAND CONTROL RUPT transfer routines. These locations are addressed as indicated below when interrupt priority control receives interrupt requests.

RPTAD12	RPTAD6	RPTAD5	RPTAD4	RPTAD3	ADDRESS	ROUTINE
1	0	0	0	1	4004	T6RUPT
1	0	0	1	0	4010	T5RUPT
1	0	0	1	1	4014	T3RUPT
1	0	1	0	0	4020	T4RUPT
1	0	1	0	1	4024	KEYRUPT
1	0	1	1	1	4034	UPRUPT
1	1	0	0	0	4040	DOWNRUPT
1	1	0	0	1	4044	RADAR RUPT
1	1	0	1	0	4050	HAND CONTROL

Inputs BBK1 through BBK3 appear on the write lines in conjunction with the contents of the erasable bank (EB) and the fixed bank (FB) registers, when both of these registers are read out simultaneously. The content of either of these registers can also be individually placed on the write lines and appear as EB9, EB10 or FB11 through FB16 respectively.

Control pulse R6 is generated as a function of peripheral instruction FETCH, and causes address 00006 to be generated to address EB and FB registers.

Octal address 00015 is placed on the write lines by control pulse R15 which is generated during instructions RUPT and RSM. During an interrupt program (RUPT), the address of the instruction to be executed next and which is stored in register Z, is transferred to location 00015 in erasable memory. When the interrupt program is completed, the resume instruction (RSM) generates control pulse R15 which in turn produces address 0015. The information entered into this location in memory during RUPT is returned to the central processor.

The quantity minus one is placed on the write lines by control pulse R1C, which is applied to write amplifiers 2 through 16. There is no connection to write amplifier 1. This action results in the quantity 1 111 111 111 111 110 (177776_8) when R1C is generated.

Control pulse RB1 is generated during certain subinstructions and causes the quantity plus one (000001_8) to be placed on the write lines. Similarly, the quantity plus two (000002_8) is placed on the write lines by control pulse RB2.

Control pulse RSTRT produces the start address when instruction GO is generated by signal GOJAM. The start address is in fixed memory at location 04000, which is determined by RSTRT as a ONE in bit 12.

Data from the IN/OUT channels is routed through the write amplifiers as inputs CH01 - CH14 and CH16.

A 16 bit word can be loaded into the LGC from the CTS during tests through inputs MDT01 through MDT16.

4-5.5.12 Register S. Register S, the memory address register, accepts the 12 bit relevant address contained in an address word. The address is written into register S (figure 4-154) from the write lines subject to write pulse $\overline{\text{WSG}}$ which is generated when control pulse $\overline{\text{WS}}$ and timing signal $\overline{\text{WT}}$ are coincident. No read signal is generated to read the address out of register S. The outputs (S01 through S12) and their complements are available directly from the output gates. Ten bit positions are used to select the first 1024 storage locations in erasable memory. All 12 bit positions are used in conjunction with three bit positions of register EBANK to select the remaining 1024 storage locations in erasable memory. In addition, all 12 bit positions of register S, 5 bit positions of register FBANK, and 3 bit positions of register FEXT enable access to all storage locations in fixed memory.

4-5.5.13 Address Decoder. A storage location in erasable memory is selected by means of an X-Y coordinate system. There are 64 X coordinates and 32 Y coordinates. The X coordinates are controlled by selection signals XB0 through XB7 and XT0 through XT7. The Y coordinates are controlled by selection signals YB0 through YB3 and YT0 through

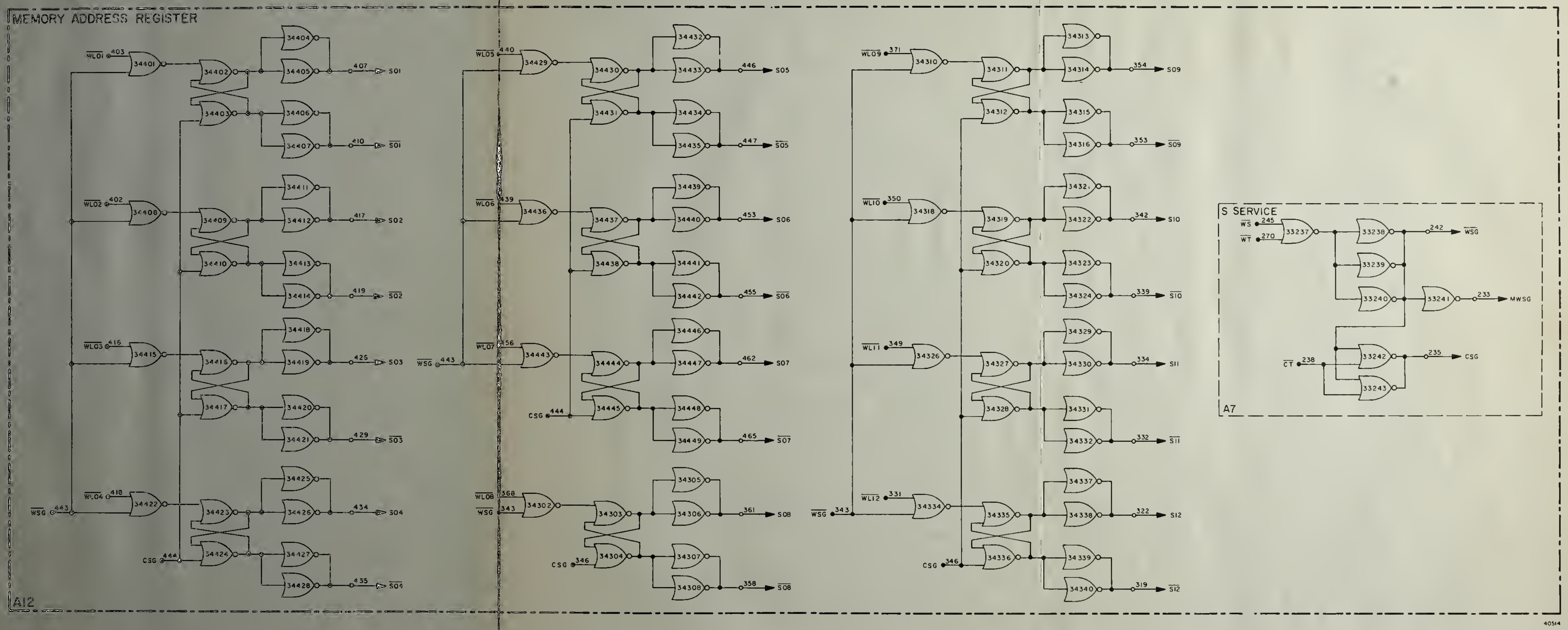

Figure 4-154. Memory Address Register (S)

YT3. Signals XB, XT, YB and YT are generated by the address decoder (figure 4-155) as a function of bits 1 through 12 from register S (S01 - S12). Bits 1 through 3 produce signals SB0 through SB7; bits 4 through 6 produce signals XT0 through XT7; bits 7 and 8 produce signals YB0 through YB3; and bits 9 and 10 in conjunction with bits EB9 through EB11 produce signals YT0 through YT7. (See table 4-LXXVIII.)

Combinations of selection signals XB, XT, YB and YT allow access to all locations in erasable memory. Signal XB, XT and YB in conjunction with signals YT0 through YT2 allow access to the first 1024 locations of erasable memory (unswitched erasable memory). Signals XB, XT, and YB in conjunction with signals YT3 through YT7 allow access to the remaining 1024 locations of erasable memory (switched erasable memory). Locations in unswitched erasable memory can also be addressed as locations of switched erasable memory if the proper bank number is entered into register EBANK. This is due to an overlap in the addressing scheme. However, addresses 0000 through 0377 (Bank 0) are normally addressed only by register S.

4-5.5.14 Counter Address Signals. Counter address signals (figure 4-156) are generated whenever counters in erasable memory must be updated. These signals are generated as a function of bits 11 and 12 of register S and address selection signals $\overline{YT0}$, $\overline{YB0}$ and $\overline{XT2}$ through $\overline{XT6}$. The address specified by these inputs must be less than 0100_8 or the generation of the counter address signals is inhibited by signal $\overline{NDR100}$.

Each counter address signal specifies certain locations in erasable memory as follows:

(1) OCTAD2 - Locations 0020 through 0027.

(2) OCTAD3 - Locations 0030 through 0037.

(3) OCTAD4 - Locations 0040 through 0047.

(4) OCTAD5 - Locations 0050 through 0057.

(5) OCTAD6 - Locations 0060 through 0067.

These output signals are supplied to priority control to prepare the priority cells to accept new incremental information.

4-5.5.15 Parity Logic. The parity logic (figure 4-157) insures that all words transferred from memory to the central processor are read out correctly and generates a parity bit for all words written into erasable memory. Parity check in the LGC is that of odd parity; that is, the total number of ONE's in the word including the parity bit is odd.

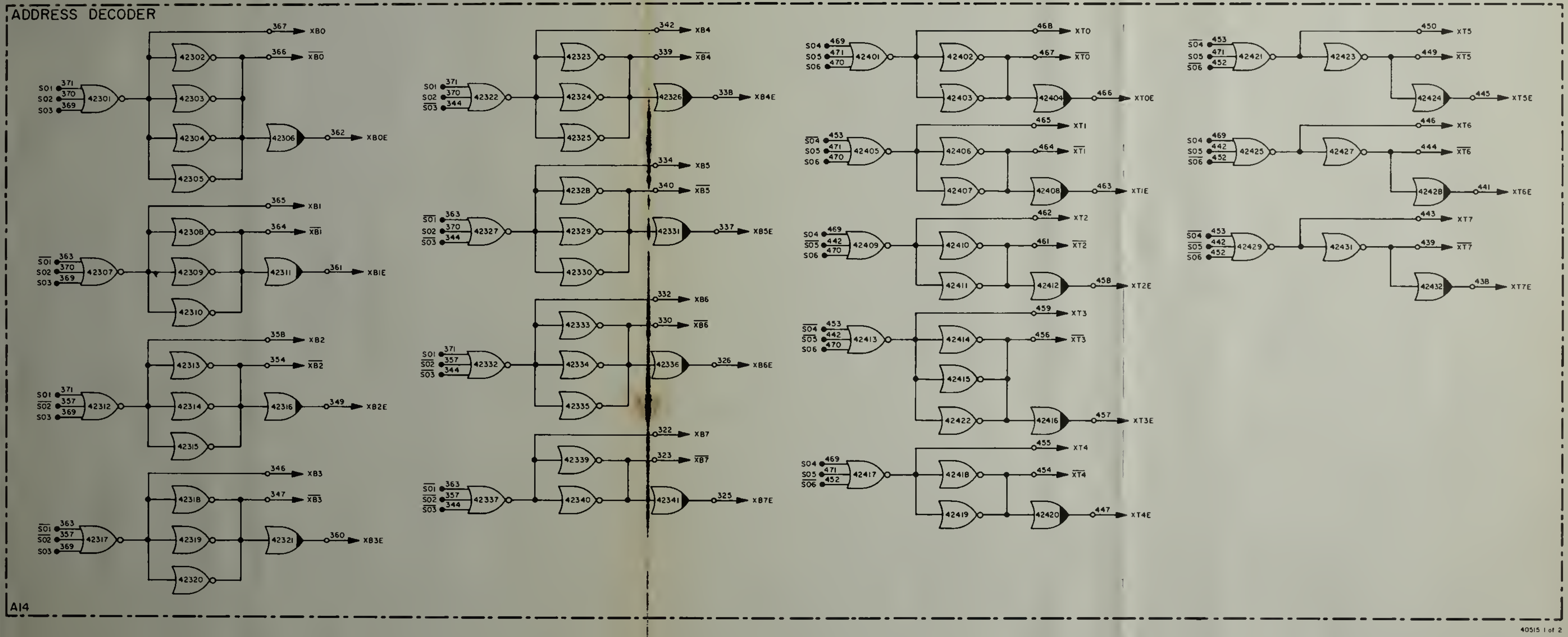

Figure 4-155. Address Decoder (Sheet 1 of 2)

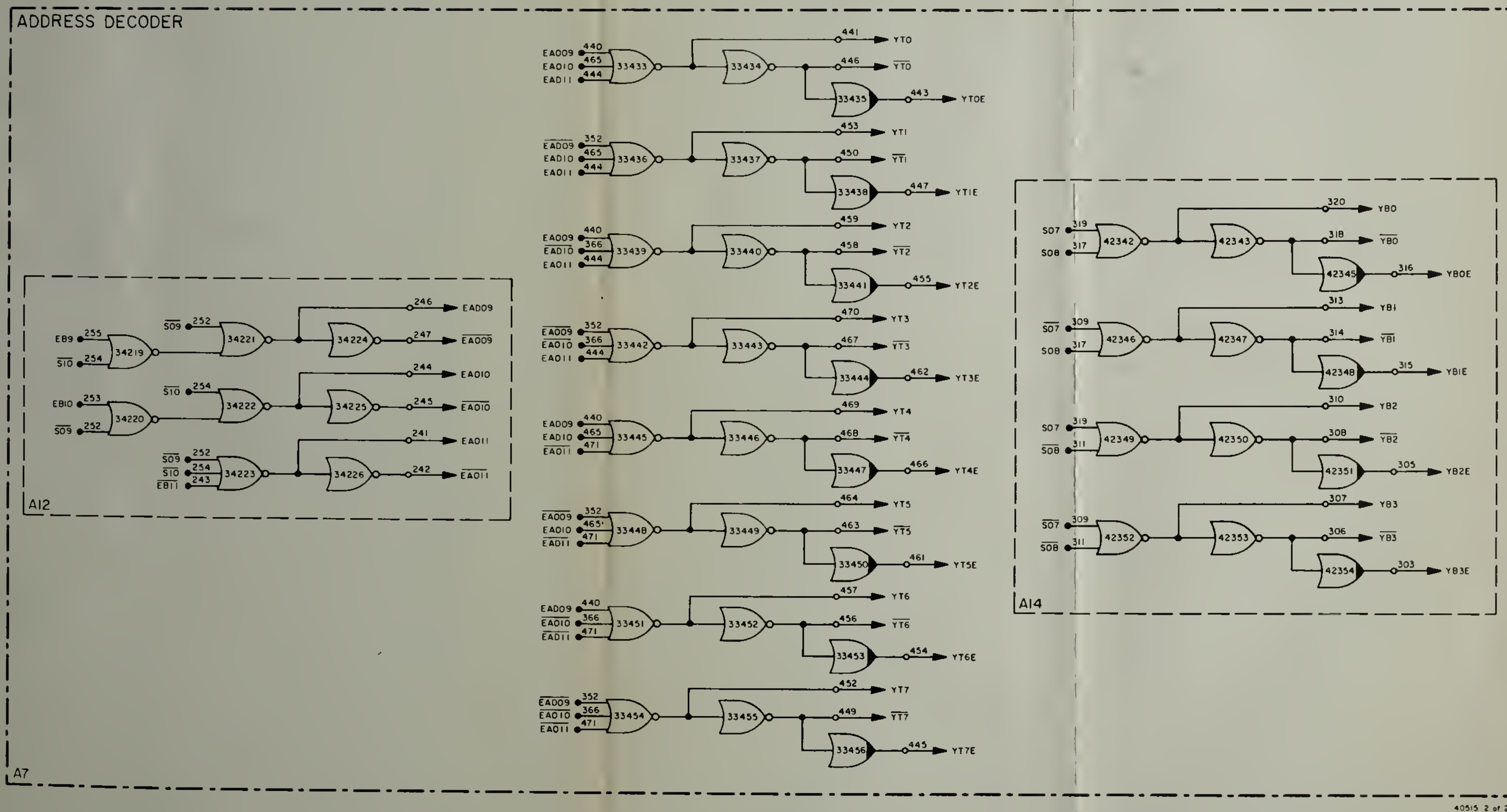

Figure 4-155. Address Decoder (Sheet 2 of 2)

Table 4-LXXVIII. Erasable Memory Address Selection

Unswitched Erasable Memory

Address	Register S Bits 12 11 10	9 8 7	6 5 4	3 2 1	Address Selection Signals
0 0 0 0 0 0 0 7	0 0 0 0 0 0	0 0 0 0 0 0	0 0 0 0 0 0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	YT0 YB0 XT0 XB0 ↓ XB7
0 0 1 0 0 0 7 7	0 0 0 0 0 0	0 0 0 0 0 0	0 0 1 1 1 1	0 0 0 1 1 1	YT0 YB0 XT1 ↓ XT7 XB0 ↓ XB7
0 1 0 0 0 3 7 7	0 0 0 0 0 0	0 0 1 0 1 1	0 0 0 1 1 1	0 0 0 1 1 1	YT0 YB1 ↓ YB3 XT0 ↓ XT7 XB0 ↓ XB7
0 4 0 0 0 7 7 7	0 0 0 0 0 0	1 0 0 1 1 1	0 0 0 1 1 1	0 0 0 1 1 1	YT1 YB0 ↓ YB3 XT0 ↓ XT7 XB0 ↓ XB7
1 0 0 0 1 3 7 7	0 0 1 0 0 1	0 0 0 0 1 1	0 0 0 0 0 0	0 0 0 0 0 0	YT2 YB0 ↓ YB3 XT0 ↓ XT7 XB0 ↓ XB7

Switched Erasable Memory

Bank	Address	E Bank Bits 11 10 9	Register S Bits 12 11 10	9 8 7	6 5 4	3 2 1	Address Selection Signals
0	1 4 0 0 1 7 7 7	0 0 0 0 0 0	0 0 1 0 0 1	1 0 0 1 1 1	0 0 0 1 1 1	0 0 0 1 1 1	YT0 YB0 ↓ YB3 XT0 ↓ XT7 XB0 ↓ XB7
1	1 4 0 0 1 7 7 7	0 0 1 0 0 1	0 0 1 0 0 1	1 0 0 1 1 1	0 0 0 1 1 1	0 0 0 1 1 1	YT1 YB0 ↓ YB3 XT0 ↓ XT7 XB0 ↓ XB7
2	1 4 0 0 1 7 7 7	0 1 0 0 1 0	0 0 1 0 0 1	1 0 0 1 1 1	0 0 0 1 1 1	0 0 0 1 1 1	YT2 YB0 ↓ YB3 XT0 ↓ XT7 XB0 ↓ XB7
3	1 4 0 0 1 7 7 7	0 1 1 0 1 1	0 0 1 0 0 1	1 0 0 1 1 1	0 0 0 1 1 1	0 0 0 1 1 1	YT3 YB0 ↓ YB3 XT0 ↓ XT7 XB0 ↓ XB7
4	1 4 0 0 1 7 7 7	1 0 0 1 0 0	0 0 1 0 0 1	1 0 0 1 1 1	0 0 0 1 1 1	0 0 0 1 1 1	YT4 YB0 ↓ YB3 XT0 ↓ XT7 XB0 ↓ XB7
5	1 4 0 0 1 7 7 7	1 0 1 1 0 1	0 0 1 0 0 1	1 0 0 1 1 1	0 0 0 1 1 1	0 0 0 1 1 1	YT5 YB0 ↓ YB3 XT0 ↓ XT7 XB0 ↓ XB7
6	1 4 0 0 1 7 7 7	1 1 0 1 1 0	0 0 1 0 0 1	1 0 0 1 1 1	0 0 0 1 1 1	0 0 0 1 1 1	YT6 YB0 ↓ YB3 XT0 ↓ XT7 XB0 ↓ XB7
7	1 4 0 0 1 7 7 7	1 1 1 1 1 1	0 0 1 0 0 1	1 0 0 1 1 1	0 0 0 1 1 1	0 0 0 1 1 1	YT7 YB0 ↓ YB3 XT0 ↓ XT7 XB0 ↓ XB7

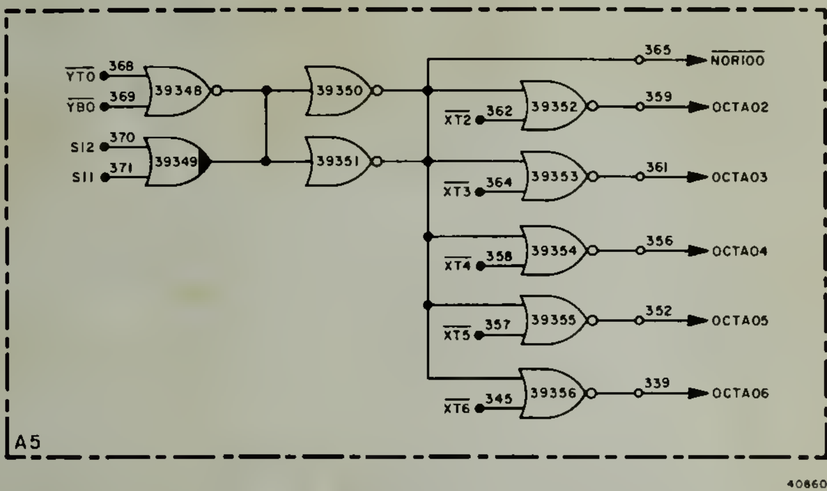

Figure 4-156. Counter Address Signals

A word read out of memory is applied directly to the parity logic from the bit outputs of register G (G01-G14 and G16), excluding bit 15, the parity bit, which is never placed on the write lines. The input gating complex of the parity logic combines the 15 bit input into a 5 bit output. The five bits are indicative of the inputs combined: PA03 indicates bits 1, 2, and 3; PA06, bits 4, 5 and 6; PA09, bits 7, 8, and 9; PA12, bits 10, 11 and 12; and PA15, bits 13, 14, and 16. The five bits are also indicative of the number of ONE's in each three bits and the total number of ONE's in the word. If any bit (PA03, PA06, etc.) is ZERO, an odd number of ONE's was contained in the three bits combined; if any is a ONE, an even number of ONE's was contained in the three bits combined. Likewise, if the 5 bit combination contains an odd number of ONE's, the entire word contained an odd number of ONE's and vice versa.

The five bit outputs and complements are applied to the parity tree (gates 34227, etc.). The inputs (PA03, PA06, etc.) are combined in this gating complex into a single output from gate 34240. This output is inverted by gate 34242.

The parity bit from memory (SAP) is applied to FF34245-34246. If the parity bit is a ONE, the flip-flop is set; if the parity bit is a ZERO, the flip-flop remains reset. The set and reset outputs of the flip-flop gate against the outputs of gates 34240 and 34242, respectively. If parity is correct, no alarm occurs; a parity error generates a parity alarm signal (PAL E).

When a word is to be written into erasable memory, the parity logic generates a parity bit and writes this bit into memory. This is accomplished as follows: A word being written into memory is deposited in register G. Simultaneously, the bit outputs of G are applied to the parity logic. The word is checked for an even or odd number of ONE's, and PAL E occurs in case of incorrect parity. The parity tree output is applied to gate 34243. This output (PC15) is the correct parity bit of the word. The parity bit is applied directly to memory as signal GEM15.

4-5.6 PRIORITY CONTROL. Priority control (figure 4-158) consists of three separate and functionally independent areas: the start instruction control, the interrupt instruction control, and the counter instruction control. The start instruction control restarts the computer following a hardware or program failure. The interrupt instruction control forces the execution of the interrupt instruction RUPT to interrupt the current operation of the computer in favor of a programmed operation of higher priority. The counter instruction control updates counters in erasable memory upon the reception of certain incremental pulses.

4-5.6.1 Start Instruction Control. The start instruction control consists of the logic alarms processor and the start-stop generator. The logic alarms processor detects the presence of any one of several abnormal conditions that may occur within the computer, and generates an alarm signal (ALGA) whenever any of these conditions exist. The abnormal conditions are:

(1) RUPT lock

(2) TC trap

(3) Parity alarm

(4) Night watchman fail.

A RUPT lock alarm indication occurs if a program interrupt has been in progress too long, or if an interruption has not occurred during a predetermined period. The latter is indicated by the presence of the interrupt in progress signal (IIP) from the sequence generator. A TC trap alarm indication occurs if too many TC or TCF instructions are executed, or if instruction TCF or increment signal (INKL) is not executed often enough. A parity alarm occurs if a word entered into the central processor from memory has been incorrectly read out. A night watchman fail indication occurs if the computer fails to address location 0067 within a period varying from 0.64 to 1.92 sec.

The start-stop generator receives signal ALGA and generates signal GOJAM at the next time 12 to restart the computer. The restart condition is indicated on the DSKY by the RESTART lamp being lighted. The start-stop generator simultaneously produces the T12 STOP signal which inhibits the generation of timing pulses $\overline{T01}$ through $\overline{T12}$ in the timer until signal GOJAM has reset all critical circuits in the computer, and forces the sequence generator to execute instruction GO. Alarm signal START1 or START2 also causes the computer to be restarted in response to a power

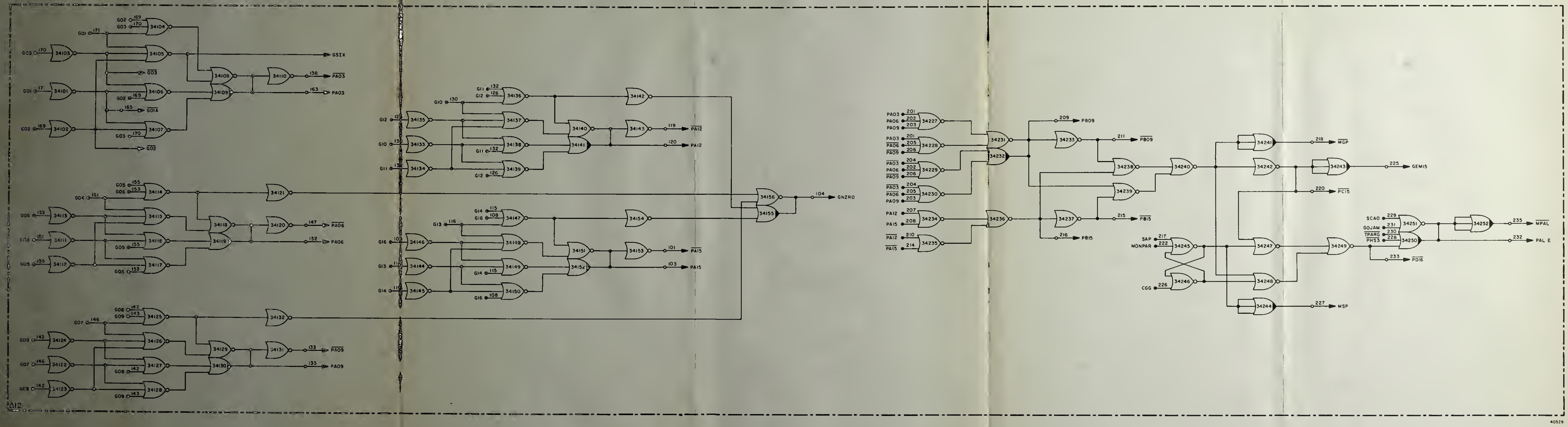

Figure 4-157. Parity Logic

supply fail or an oscillator fail, respectively. In addition, the computer can be started or stopped manually from the peripheral equipment by signals monitor start and monitor stop. Signal monitor start coincident with timing pulse $\overline{T12}$ causes the generation of signal GOJAM and signal monitor stop coincident with $\overline{T12}$ inhibits the generation of timing pulses $\overline{T01}$ through $\overline{T12}$ until the monitor stop signal is removed.

4-5.6.2 Interrupt Instruction Control. The interrupt instruction control which consists of interrupt input circuits and an interrupt address generator is used to generate an interrupt address and the interrupt order code signal (RUPTOR) when interrupt control signals (requests) are received from the input-output section. The 12-bit interrupt address causes the addressing of one of ten locations in fixed memory dependent upon the interrupt request received. These ten locations contain the first instruction of a RUPT transfer subroutine which, when executed, initiates the execution of a particular routine within the program.

The interrupt input circuits receive interrupt control signals from the input-output section and decoded addresses from the central processor. From these inputs, the input circuits generate interrupt requests and priority signals subject to control pulses from the sequence generator. The interrupts are processed on a priority basis such that those interrupts having the highest priority (lowest priority number) are processed first. The priority signals specify the priority of the interrupt being processed. The interrupts and their respective priorities are as follows:

Priority	Interrupt
1	T6RUPT
2	T5RUPT
3	T3RUPT
4	T4RUPT
5	KYRPT
6	UPRUPT
7	DLKRPT
8	HNDRPT

The first four interrupts (T6RUPT, T5RUPT, T3RUPT and T4RUPT) occur when their respective time counters overflow while being incremented. A T6RUPT enables information to be sent to the RCS; a T5RUPT enables information to be sent to the SCS; a T3RUPT enables the computer to perform internal tasks that must be performed at a specific time; and a T4RUPT enables information to be sent to the DSKY, the ISS, and the LORS. The keycode interrupt (KYRPT) occurs when any key is pressed on the DSKY. An UPRUPT is generated when the flag bit appears in bit position 16 of the uplink word which indicates that the serial-to-parallel conversion is complete. A DLKRPT is generated when the downlink end pulse is received indicating the end of a downlink transmission. This interrupt allows the appropriate output channel to be loaded in preparation for the next downlink transmission. A HNDRPT occurs whenever a command is received from the hand controllers in the spacecraft.

The interrupt address generator receives interrupt requests and priority signals and generates the address of the first location of the appropriate interrupt transfer subroutine. The addresses and the associated interrupt transfer subroutines are:

Address	Subroutine
4004	T6RUPT
4010	T5RUPT
4014	T3RUPT
4020	T4RUPT
4024	KEYRUPT
4034	UPRUPT
4040	DOWNRUPT
4050	HAND CONTROL RUPT.

The interrupt address generator produces signal RUPTOR which is supplied to the sequence generator to cause the generation of instruction RUPT. Thus, when an interrupt condition occurs, the priority of the request is generated which inhibits the generation of lower priority interrupts, the address of the interrupt transfer subroutine is formed, and the sequence generator is conditioned to interrupt the normal program operation to allow the interrupt to be processed. The interrupt address is then supplied to the interrupt input circuits to reset them in preparation for the next interrupt.

4-5.6.3 Counter Instruction Control. The counter instruction control receives incremental pulses from the input-output section to update the various counters in erasable memory (locations 0024 through 0060). Counter instruction control consists of counter priority cells, a counter alarm detector, and a counter address generator. There are 29 priority cells in the counter instruction control, one cell per counter. When an incremental pulse is received, the appropriate priority cell generates an address signal and a counter instruction signal. The address signal enables the counter address generator to form the address of the counter to be updated and the counter instruction signal forces the sequence generator to generate counter instructions (PINC, MINC, SHINC, SHANC, PCDU and MCDU). Those priority cells associated with counters requiring only one counter instruction (such as PINC or MINC) generate only one instruction signal. Those cells associated with counters requiring two counter instructions (such as PINC and MINC) generate two instruction signals.

The counters in memory are updated according to a priority scheme in which the counter having the lowest address has the highest priority and the counter having the highest address has the lowest priority. When a particular counter is being updated, all other counters of lower priority are inhibited from being updated by the priority cells. In addition, the priority cells generate a counter OR (CTROR) signal which is supplied to the sequence generator and the counter alarm detector. This signal is used in the sequence generator to produce increment signal INKL which must be generated prior to a counter instruction.

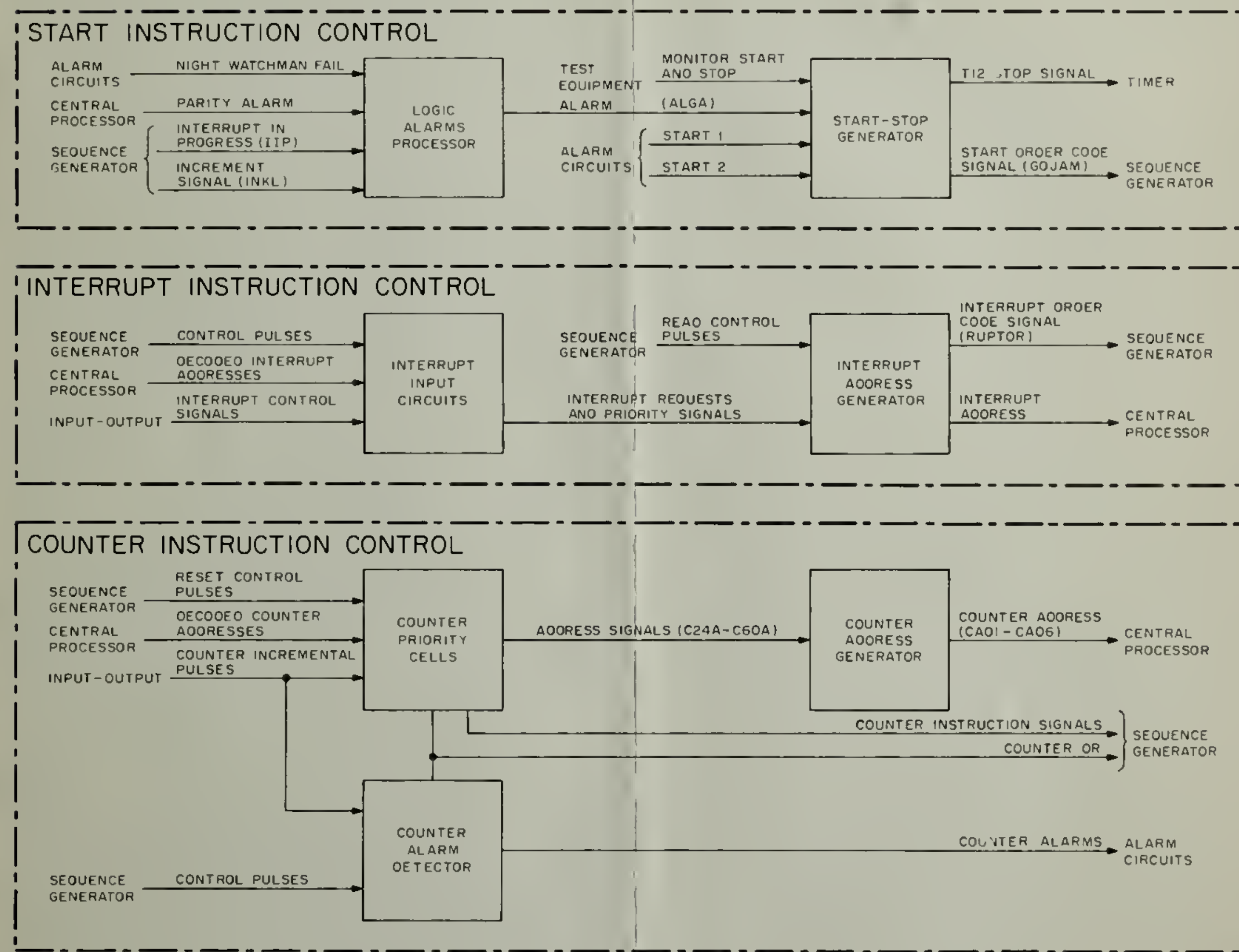

Figure 4-158. Priority Control Functional Block Diagram

The counter address generator receives address signals from the priority cells and generates the address of the counter to be updated. This address is contained in six bits (CAD1 through CAD6) which are the six least significant bits; however, it produces a 12 bit address in the central processor since the six most significant bits contain ZERO's when placed on the write lines. When the counter address is supplied to memory by the central processor, it is also supplied to the counter priority cells. This address in conjunction with reset control pulses from the sequence generator resets the priority cell that generated the address signal in preparation for the next incremental pulse.

Counter incremental pulses are also supplied to the counter alarm detector to insure the detection of abnormal counter activity. A counter alarm is generated if a counter is not updated following the generation of an increment request (INKL) by the sequence generator, or if a counter increment lasts too long (over 0.625 msec). The counter alarm is forwarded to the alarm circuits to initiate a failure display.

4-5.7 INPUT-OUTPUT. The input-output section consists basically of the interface circuits and the input and output channels. This functional area is the means by which information is transferred between the LGC and the other LEM systems.

4-5.7.1 Input-Output Functional Description. The interface circuits accept all inputs to and route all outputs from the computer. This portion of the input-output section contains a variety of circuits which provide the necessary voltage levels or electrical isolation of the input and output signals. Incremental inputs as well as serial pulse inputs are applied through input transformer circuits. All discrete inputs such as the keycodes from the DSKY are applied through resistive-capacitive networks. Incremental output drive pulses such as those to the gyros and CDU, and serial pulse outputs are applied through output transformer circuits. Timing and synchronization pulse trains to other LEM systems are likewise applied through output transformer circuits. Discrete outputs are applied through output transistor driver circuits. Power outputs (+28 COM, +4, +14 volts) are supplied through isolation resistors located in the interface circuits. Most of the input signals to the LGC are applied to the input channels; likewise, the source of most of the output signals is the output channel network. The remaining inputs and outputs are applied to or come from other functional areas within the computer.

There are six input channels and eight output channels which interface with other spacecraft systems and the DSKY (figure 4-159). A ninth output channel (7) functions internally in the LGC to address fixed memory. The address of the channels is the same as the channel number (channel 30 - address 0030). Input channels 15 and 16 are flip-flop registers similar to the flip-flop registers of the central processor. Channels 30 through 33 each consist of an input gating complex to which discrete inputs are applied. The channels are interrogated under program control by a set of channel

instructions. An address, supplied by program, is applied to the service gates of an associated channel and the data in that channel is readout to the central processor. The numbers used to address both the input and output channels coincide with some of the numbers used as memory addresses. However, the addresses used for the input and output channels are supplied by the IN/OUT instruction group and are always channel addresses. The addresses in other instructions are always memory addresses. This coincidence of addresses can make two registers accessible in the central processor. Register L is accessible both at memory address 001 and channel address 01; register Q is accessible at memory address 0002 and channel address 02. There is no write process involved with the input channels as is the case with the flip-flop registers of the central processor, however. Inputs are entered directly into the bit positions of the channels. The number of bits in parentheses of each channel block in figure 4-159 indicates the number of active bit positions. All channels have a capacity of 15 bits.

The inputs into the input channels are all discrete inputs. These can be further classified into interrupting and non-interrupting. The keyboard and LORS discrete inputs into channels 15 and 16 are the only two interrupting discrete type inputs. That is, a keycode input from the DSKY into channel 15, or a LORS discrete input to channel 16 interrupts the program being executed and forces the computer to interrogate that particular channel. This is accomplished by an interrupt signal which is generated simultaneously as the inputs enter channel 15 or 16. The inputs into the remaining channels from the various other LEM systems as indicated are non-interrupting. The channels are interrogated by program, as described previously, and the information is readout to the central processor.

Incremental inputs representing velocity changes are applied directly from the interface circuits to the PIPA precount logic. From this logic section, incremental pulses are applied to priority control to initiate a counter interrupt routine, and update an associated counter in memory. In a similar manner, the incremental inputs from the CDU representing the gimbal angles of the ISS and LORS are applied directly to priority control and initiate a counter interrupt routine.

Channel 13 (figure 4-160) controls the serial inlink inputs to the LGC, the downlink transmission, the BMAG inputs (body mounted attitude gyros), and functions internal to the LGC. The channel bit positions are enabled by program control. Information is entered into the respective bit positions from the central processor. Bits 1 through 4 of channel 13 control outputs to the radar. Inlink consists of the uplink word from spacecraft telemetry (used only in unmanned flights) and the crosslink word from the CMC. Normally, the uplink data is entered into the input circuits and subsequently to priority control to initiate a counter interrupt. A ONE entered into bit position 5 of channel 13 from the central processor inhibits uplink and enables the crosslink input from the CMC to the LGC. Uplink information can also be inhibited by the BLOCK UPLINK signal. Bit 6 of channel 13 inhibits any inlink (uplink or crosslink) information from entering the computer. Bit 7 controls the word order gate in the downlink logic, which is discussed under the output channel logic. The BMAG inputs are applied to

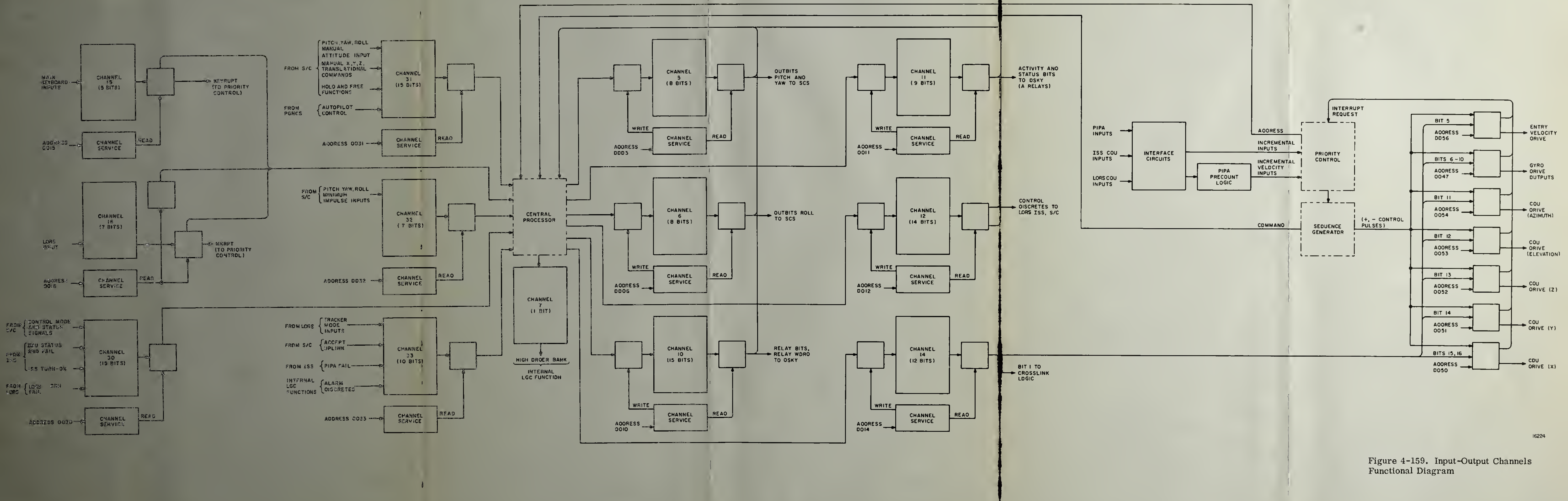

Figure 4-159. Input-Output Channels Functional Diagram

priority control as a function of bit 8. A ONE entered into this bit position of channel 13 allows these incremental inputs to initiate a counter interrupt sequence in priority control and update an associated counter in memory. Bits 10, 11, and 15/16 of channel 13 are control bits for functions internal to the LGC. Bit 10 (Alarms Test) lights the RESTART and STBY lamps on the DSKY. Bit 11 enables the LGC to enter the standby mode. Bit 15/16 enables the T6 interrupt routine. The manual inputs entered into channel 31 (attitude and translational) initiate an interrupt sequence under program control through bits 12 and 13 of channel 13. Thc manual discrete inputs are applied to the handrupt control logic. The program enters the proper data into positions 12 and/or 13 and HNDRPT is initiated.

The output channels (figure 4-159) are all flip-flop registers with write and read service. Data is written into the output channels from the central processor coincident with an address supplied by the program into the service gates. Output channels 5, 6, 10, 11, and 12 supply output discretes to other systems as indicated in figure 4-159. Channel 14 controls the transmission of incremental drive pulses to the gyros and the CDU. An output is enabled (gyro or CDU) by placing a ONE in the proper bit position of channel 14. This is accomplished by the program. For example, the program enters a ONE into bit position 11 of channel 14. This results in an interrupt request signal which is applied to priority control. Further processing by priority control results in a command request to the sequence generator and an address command to the central processor. This same address (in this case 0054) enables the output drive logic and allows the drive pulses to be gated out. The associated output counter register in memory is loaded by program and a pulse burst is sent to the CDU. Each time the counter is processed the number in the counter register is diminished by one such that the content of the counter approaches zero. When the number has reached zero, the channel bit position is reset and the pulse burst terminates.

The outlink control logic is functionally illustrated in figure 4-161. Outlink consists of the downlink word to the spacecraft telemetry, and the crosslink word to the CMC. The word to be transmitted downlink is loaded into channel 34 from the central processor. DLKRPT is initiated by the downlink rupt circuit. DKSTRT is converted to a clear pulse to clear the downlink counter, and also sets the read flip-flop. The bit sync pulses then step the counter and the outputs are decoded to strobe the bit positions of channel 34, and produce a serial word output. The rate of transmission is monitored, and, if too fast, a bit is entered into bit position 12 of channel 33. Crosslink is the output word from the LGC to the CMC. Bit 1 of channel 14 enables the outlink control logic. An interrupt request signal is sent to priority control to initiate an interrupt sequence. The address of the crosslink counter enables the word from the central processor to be transmitted serially to the CMC.

4-5.8 MEMORY. Memory consists of an erasable memory with a storage capacity of 2048 words and a fixed core rope memory with a storage capacity of 36,864 words. Erasable memory is a random-access, destructive readout storage device. Data stored in erasable memory can be altered or updated. Fixed memory is a nondestructive storage device. Data stored in fixed memory is unalterable since the data is wired in.

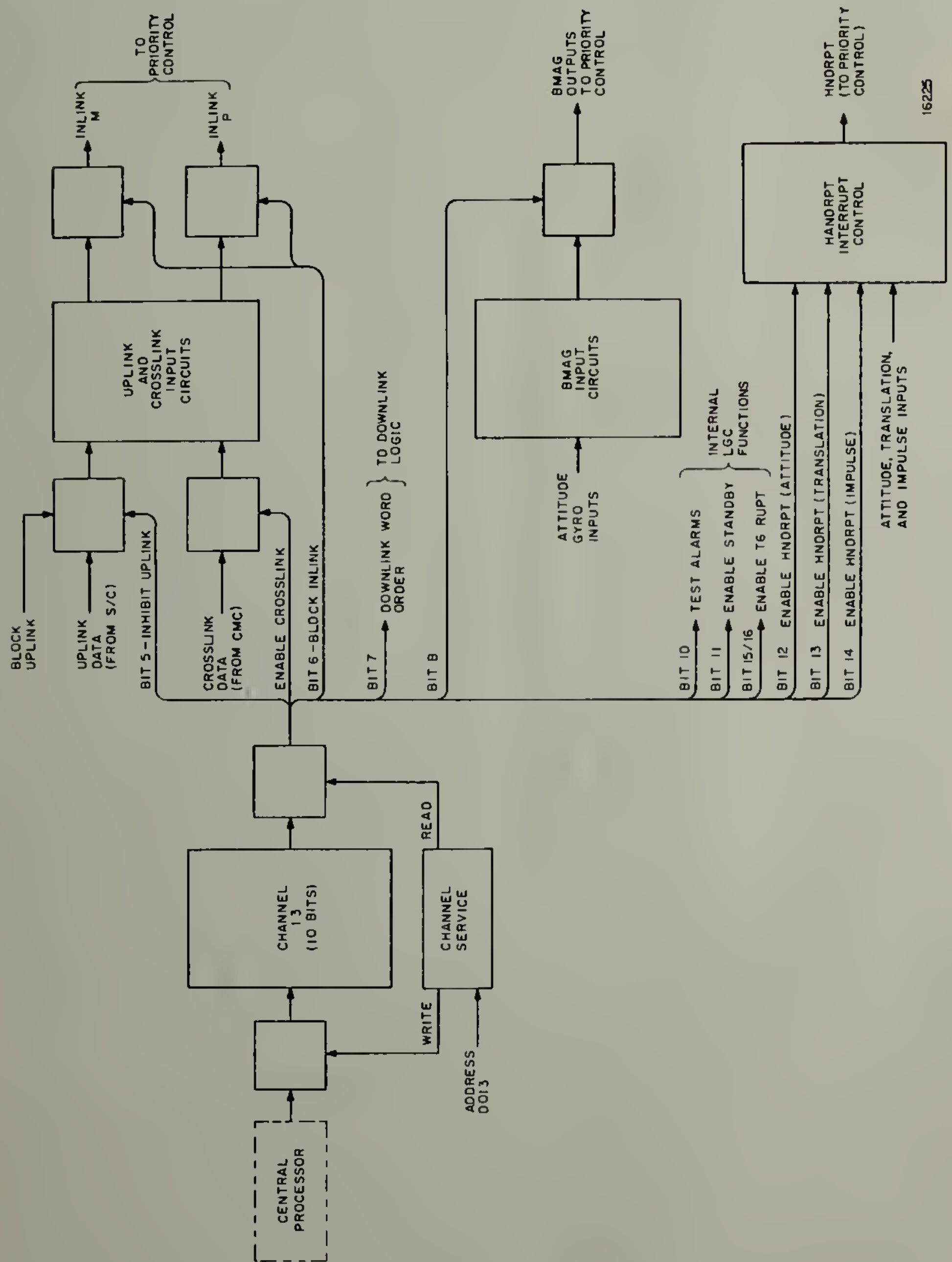

Figure 4-160. Inlink Functional Diagram

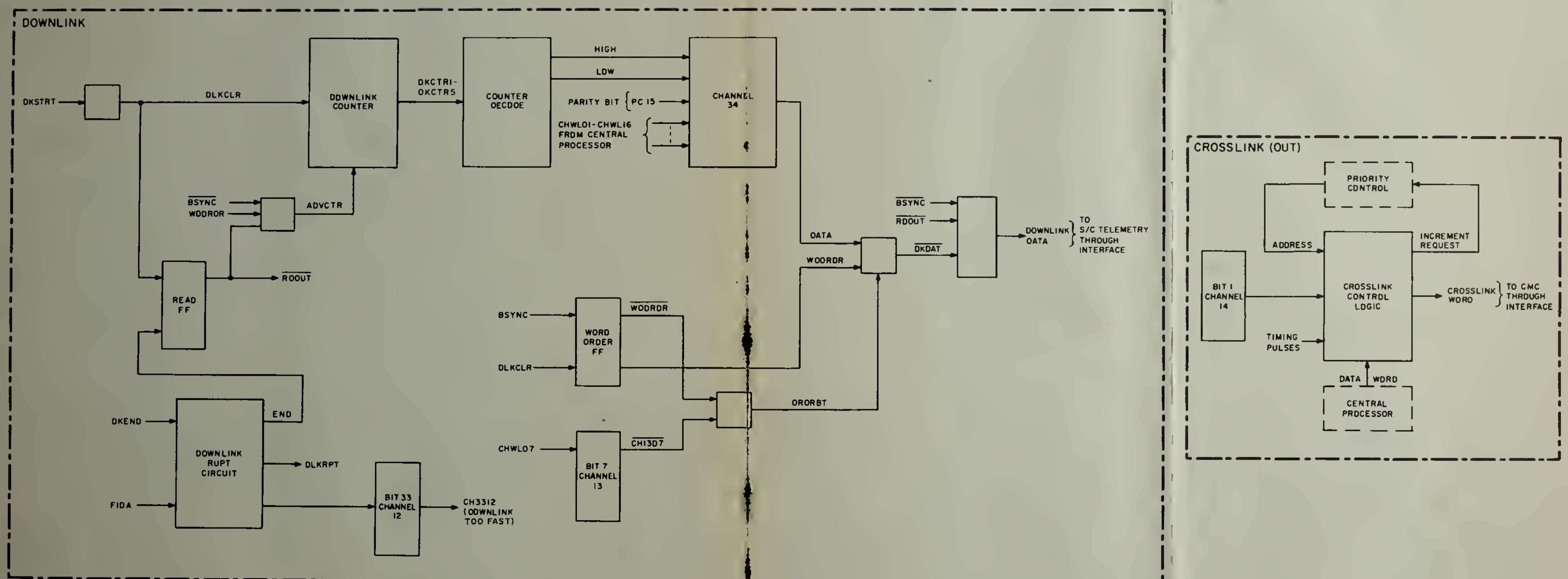

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Figure 4-161. Outlink Functional Diagram

Both memories contain magnetic-core storage elements. In erasable memory the storage elements form a core array (one module); in fixed memory the storage elements form three core ropes (six modules). Erasable memory has a density of one word per 16 cores; fixed memory has a density of twelve words per core. Each word is located by an address from the central processor.

4-5.8.1 Erasable Memory Functional Description. Erasable memory (figure 4-162) consists of a core array, memory cycle timing circuits, selection circuits, and sense amplifiers. The core array is the medium by which data is stored in erasable memory. The memory cycle timing circuits generate strobe signals which enable the selection circuits and the sense amplifiers. The selection circuits select the addressed storage location under control of the selection signals from the address decoder in the central processor and strobe signals from the memory cycle timing circuits. The sense amplifiers detect the contents of the selected storage location and supply this data to register G.

Erasable memory is addressed (table 4-LXXIX) by the contents of registers S and EBANK of the central processor. Erasable memory is subdivided into eight banks (0 through 7), each storing 256 words. The first 8 locations of bank 0 are used for addressing the central processor registers. Another 12 addresses are reserved for addressing special locations and 29 for addressing counters. The remaining 207 addresses of bank 0 are used for addressing locations which are accessible for general use.

Banks 0, 1, and 2 are referred to as unswitched E memory because all their locations can be addressed by register S without regard to what might be contained in EBANK. Banks 3 through 7 are referred to as switched E memory because their locations can be addressed only through a combination of the S and EBANK registers. Locations in unswitched E memory can also be addressed as locations in switched E memory if the proper bank address is contained in register EBANK.

Erasable memory is addressed only when bit positions 12 and 11 of register S are logic ZERO's. When bit positions 10 and 9 also contain ZERO's it indicates that a location in bank 0 is addressed, regardless of the contents of register EBANK. When bit 10 or 9, but not both contain a ONE, a location in bank 1 or 2 is addressed regardless of the contents of register EBANK. When bit positions 10 and 9 both contain a ONE, a location is addressed in that bank, the number of which is contained in register EBANK.

4-5.8.1.1 Core Array. The core array of erasable memory has 2048 word storage locations, contained in 16 bit planes and defined by the intersection of 64 X lines and 32 Y lines. Each bit plane contains 2048 cores. An individual bit in each plane is selected by the intersection of an X and Y line threading a core. Thus, one word storage location is selected. Each core is also threaded by a sense line and an inhibit line. The sense line threads all cores in a particular bit plane, such that current is induced into the sense line if the state of any core in the plane is changed. Current through

the inhibit line prevents any core in the bit plane from switching since it opposes the current on the X and Y selection lines. Thus, current in a combination X, Y, and inhibit lines determines which cores are selected. Core selection is identical for both the read and write operations.

4-5.8.1.2 Erasable Memory Cycle Timing Circuits. The erasable memory cycle timing circuits consist of timing control and timing flip-flops, which generate strobe signals to sequence the operation of erasable memory. These strobe signals are generated during one memory cycle time (11.97 microseconds), subject to timing signals from the timer as shown in figure 4-163. The timing flip-flops generate the strobe signals subject to signal $\overline{\text{ERAS}}$ from the timing control. Signal $\overline{\text{ERAS}}$ is generated only when bits 11 and 12 of register S in the central processor are both ZERO's, the subinstruction commands from the sequence generator are all ZERO's, and signal SCAD is not present. Bits 11 and 12 are ZERO's when the specified memory address is lower than 2000 (octal). Signal SCAD is a ONE only when the specified address is lower than 0007. The timing control also generates signal TIMR when signal $\overline{\text{STOP}}$ (represents CTS start and stop or alarm condition) is present. Signal TIMR resets several timing flip-flops in erasable memory and inhibits the addressing of the ropes in fixed memory. Input signal MYCLMP inhibits access to memory if the +4 vdc power supply fails or the LGC is in the standby mode.

The timing flip-flops generate the various strobe signals which enable the selection circuits and sense amplifiers. As previously discussed, several strobe signals are inhibited by signal TIMR and those remaining by signal GOJAM.

4-5.8.1.3 Selection Circuits. Selection signals (X and Y) from the address decoder in the central processor are applied to the top and bottom select drivers. When these drivers receive the set strobe, the selection signals are supplied to the top and bottom selection switches. The read signals (X and Y) enable the top selection switches and allow current to flow from the bottom selection switch through the core array to the top selection switches. The current flowing through the X and Y lines coincides at the addressed storage location (one core of each plane) in the core array. As a result, current is induced into the sense lines which thread those cores that switched from a ONE to a ZERO. The current on the sixteen sense lines is detected by the sense amplifiers and applied to register G when the sense strobe is generated. The selection switches remain set until the reset signals are received.

The write signals (X and Y) enable the bottom selection switches and allow current to flow from the top selection switches through the core array to the bottom selection switches. Again the current flowing through the X and Y lines coincides at the addressed location in the core array. However, during the write operation the cores in the addressed location are switched to a ONE, provided they are not also receiving current in the inhibit lines. All cores receiving inhibit current remain in a ZERO condition. Inhibit current is governed by the content of register G. There are 16 inhibit drivers, and each is connected to a bit plane. Thus, the content of register G determines which cores in a storage location are switched by the X and Y selection lines during the write operation.

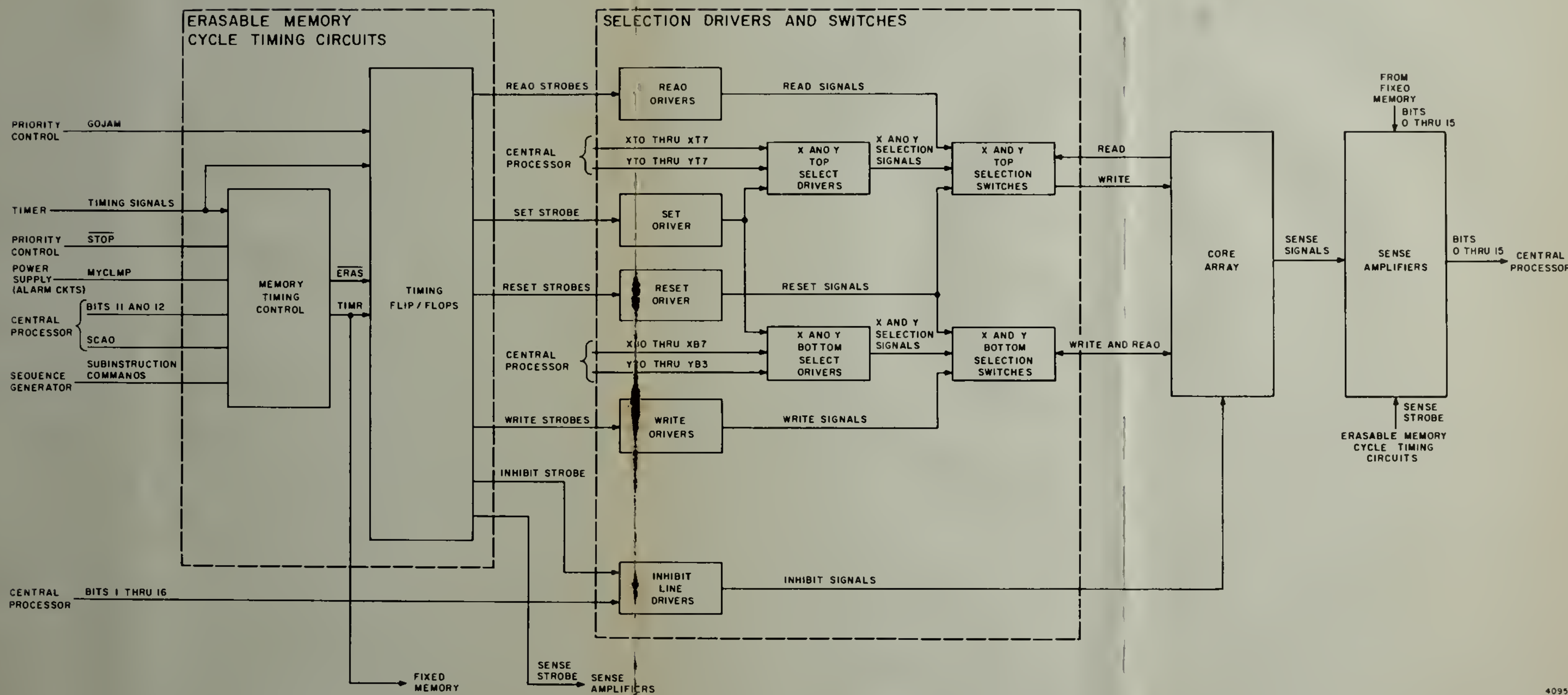

Figure 4-162. Erasable Memory Functional Diagram

Table 4-LXXIX. E Addressing

Register or Location Groups			Octal Address Pseudo	Octal Address Real	EBANK 11	EBANK 10	EBANK 9	S 12	S 11	S 10	S 9	S 8	S 7	S 6	S 5	S 4	S 3	S 2	S 1
		CP	0000-0007	0000-0007	x	x	x	0	0	0	0	0	0	0	0	0	y	y	y
				1400-1407	0	0	0	0	0	1	1	0	0	0	0	0	y	y	y
Unswitched E Memory	EBANK O	Special Locations	0010-0023	0010-0023	x	x	x	0	0	0	0	0	0	0	y	y	y	y	y
				1410-1423	0	0	0	0	0	1	1	0	0	0	y	y	y	y	y
		Counters	0024-0060	0024-0060	x	x	x	0	0	0	0	0	0	y	y	y	y	y	y
				1424-1460	0	0	0	0	0	1	1	0	0	y	y	y	y	y	y
		General Use	0061-0377	0062-0377	x	x	x	0	0	0	0	y	y	y	y	y	y	y	y
				1462-1777	0	0	0	0	0	1	1	y	y	y	y	y	y	y	y
		E-Bank 1	0400-0777	0400-0777	x	x	x	0	0	0	1	y	y	y	y	y	y	y	y
				1400-1777	0	0	1	0	0	1	1	y	y	y	y	y	y	y	y
		E-Bank 2	1000-1377	1000-1377	x	x	x	0	0	1	0	y	y	y	y	y	y	y	y
				1400-1777	0	1	0	0	0	1	1	y	y	y	y	y	y	y	y
Switched E Memory		E-Bank 3	1400-1777	1400-1777	0	1	1	0	0	1	1	y	y	y	y	y	y	y	y
		E-Bank 4	2000-2377	1400-1777	1	0	0	0	0	1	1	y	y	y	y	y	y	y	y
		E-Bank 5	2400-2777	1400-1777	1	0	1	0	0	1	1	y	y	y	y	y	y	y	y
		E-Bank 6	3000-3377	1400-1777	1	1	0	0	0	1	1	y	y	y	y	y	y	y	y
		E-Bank 7	3400-3777	1400-1777	1	1	1	0	0	1	1	y	y	y	y	y	y	y	y

⚠1 x means 0 or 1 which does not have an effect on addressing.
y means 0 or 1 as defined by address.

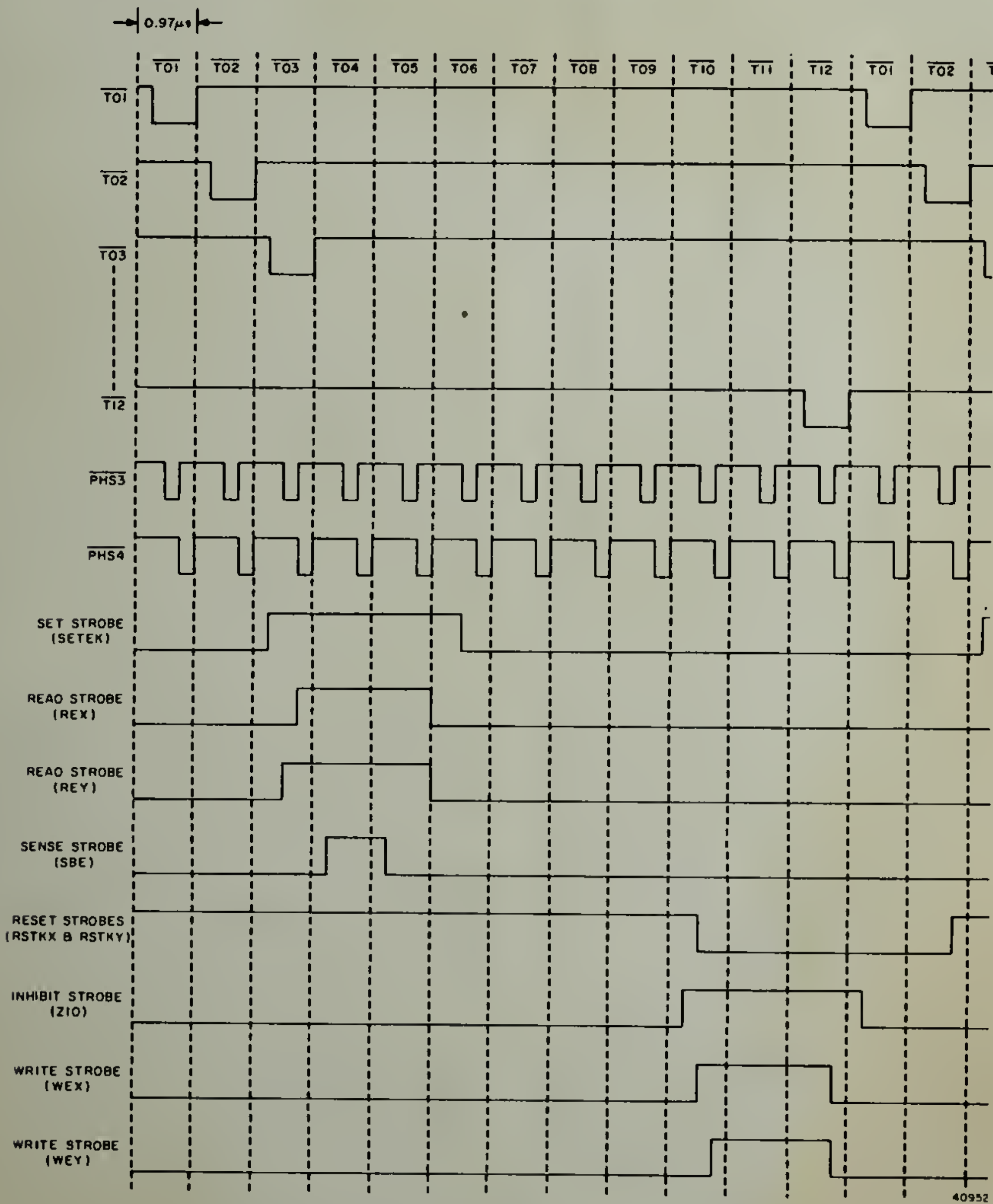

Figure 4-163. Erasable Memory Timing Diagram

Figure 4-164 is a simplified diagram of the selection circuits. Each selection signal effectively closes one top or bottom selection switch. Any one of 64 lines can be selected by closing one top and one bottom selection switch (XT and XB). Similarly any one of 32 lines can be selected by closing one top and one bottom selection switch (YT and YB). Where they intersect in the core array is the addressed location. This occurs in the same position in all sixteen bit planes of erasable memory.

4-5.8.1.4 Sense Amplifiers. There are 16 sense amplifiers in erasable memory. Each amplifier senses the content of a bit location during the read operation. The bi-polar sense signals are converted to single polarity signals and forwarded to register G when the amplifiers are enabled with the sense strobe. In addition, the word read out of fixed memory is also gated through the erasable memory amplifiers to register G.

4-5.8.2 Fixed Memory Functional Description. Fixed memory (figure 4-165) consists of fixed memory cycle timing circuits, selection circuits and drivers, core ropes and return circuits, and the sense amplifiers. Memory cycle timing generates the timing signals necessary for fixed memory operation. A location in fixed memory is addressed according to the contents of registers S, FBANK, and FEXT in the central processor. The selection circuits convert the contents of registers S, FBANK, and FEXT into the various signals necessary to select the addressed storage location. The three core ropes, which are the storage medium for storing data in fixed memory, are designated ropes R, S, and T. A rope consists of two modules and each module contains 512 cores. The sense amplifiers detect the content of the addressed storage location and supply this data through the sense amplifiers in erasable memory to the central processor.

Fixed memory is subdivided into 64 banks for addressing (table 4-LXXX), each storing 1024 words. However, only 36 banks (00 through 43) are built into the LGC, but the other 28 banks (44 through 77) can be added.

Banks 00 through 27 are referred to as FEXT - Channel X because all of the locations can be addressed by entering the address in registers S and FBANK without regard to what might be contained in register FEXT. All other banks, 30 through 77, may be addressed only if the correct channel number (0-3, 4, 5, 6, or 7) is contained in register FEXT.

Banks 02 and 03 are also referred to as fixed-fixed memory because the locations can be addressed by entering the proper address in register S without regard to what might be contained in register FBANK. Banks 00, 01 and 04 through 27 are also referred to as variable fixed memory, however, the proper bank number must be contained in register FBANK.

Fixed memory is addressed only when bit position 12 or 11, or both, of register S contain a ONE. Whenever bit position 12 contains a ONE, fixed-fixed memory is addressed, regardless of the contents of registers FBANK and FEXT. Whenever bit position 12 contains a ZERO and bit position 11 a ONE, a location is addressed in that bank which is defined by the contents of registers FBANK and FEXT.

When bit positions 16 and 14 of register FBANK both contain ZERO's, or a ZERO and a ONE, bit position 12 of register S contains a ZERO, and bit position 11 a ONE, it indicates that a bank in FEXT (Channel X) is addressed, in which case the content of register FEXT is irrelevant. When bit positions 16 and 14, of register FBANK, contain ONE's, a bank in FEXT - Channel 0-3, or 4 through 77 is addressed.

4-5.8.2.1 Fixed Memory Cycle Timing Circuits. Fixed memory cycle timing consists of timing control and timing flip-flops. The timing control regulates the generation of timing signals, used for fixed memory operation, by means of signal $\overline{\text{ROP}}$. Signal $\overline{\text{ROP}}$ is generated when either bit 11 or bit 12, or both, are ONE's. Signal $\overline{\text{ROP}}$ occurs for memory addresses above 1777. The timing flip-flops generate the timing signals (figure 4-166) necessary to sequence the operation of fixed memory subject to timing signals from the timer, and subinstruction commands from the sequence generator. The timing signals generated are IHENV (enables the inhibit drivers), SET ENABLE (enables the set circuits), STRGAT (enables the rope and strand circuits), RESET ENABLE (enables the reset circuits), and STBF (enables the sense amplifiers). The generation of the inhibit and set signals is inhibited by signal TIMR from the erasable memory cycle timing circuits. The remaining timing signals are inhibited by signal GOJAM from priority control.

4-5.8.2.2 Selection Circuits and Drivers. The selection circuits generate the rope, strand, module, set, reset, and inhibit signals necessary to select an addressed storage location in fixed memory.

Set selection is accomplished by signals S09 and $\overline{\text{S09}}$ subject to the set enable timing signal. One of two set signals (SETAB or SETCD) is fed through a driver circuit and applied to the core ropes.

Reset selection is accomplished by signals S08, $\overline{\text{S08}}$, S09, and $\overline{\text{S09}}$ subject to the reset enable timing signal. One of four reset signals (RESET A, B, C or D) is fed through a driver circuit and applied to the core ropes.

Inhibit selection is divided into two parts. Signals S01 through S07 and their complements determine which of the 14 inhibit lines is activated, and the remaining two lines are activated by X and Y selection signals from erasable memory. The inhibit lines are applied to the core ropes subject to timing signal IHENV.

The rope and strand selection is accomplished by combining signals S10 and $\overline{\text{S10}}$ with signals F11 through F16 and their complements. Module selection is accomplished by combining the rope and strand selection signals.

A rope is selected by applying one of three rope selection signals to a particular rope return circuit. The sense lines threading or bypassing each core are grouped together into strands. A particular sense strand (1 of 72) is selected and applied to the core ropes. Module selection allows one module of the six in the core ropes to be activated.

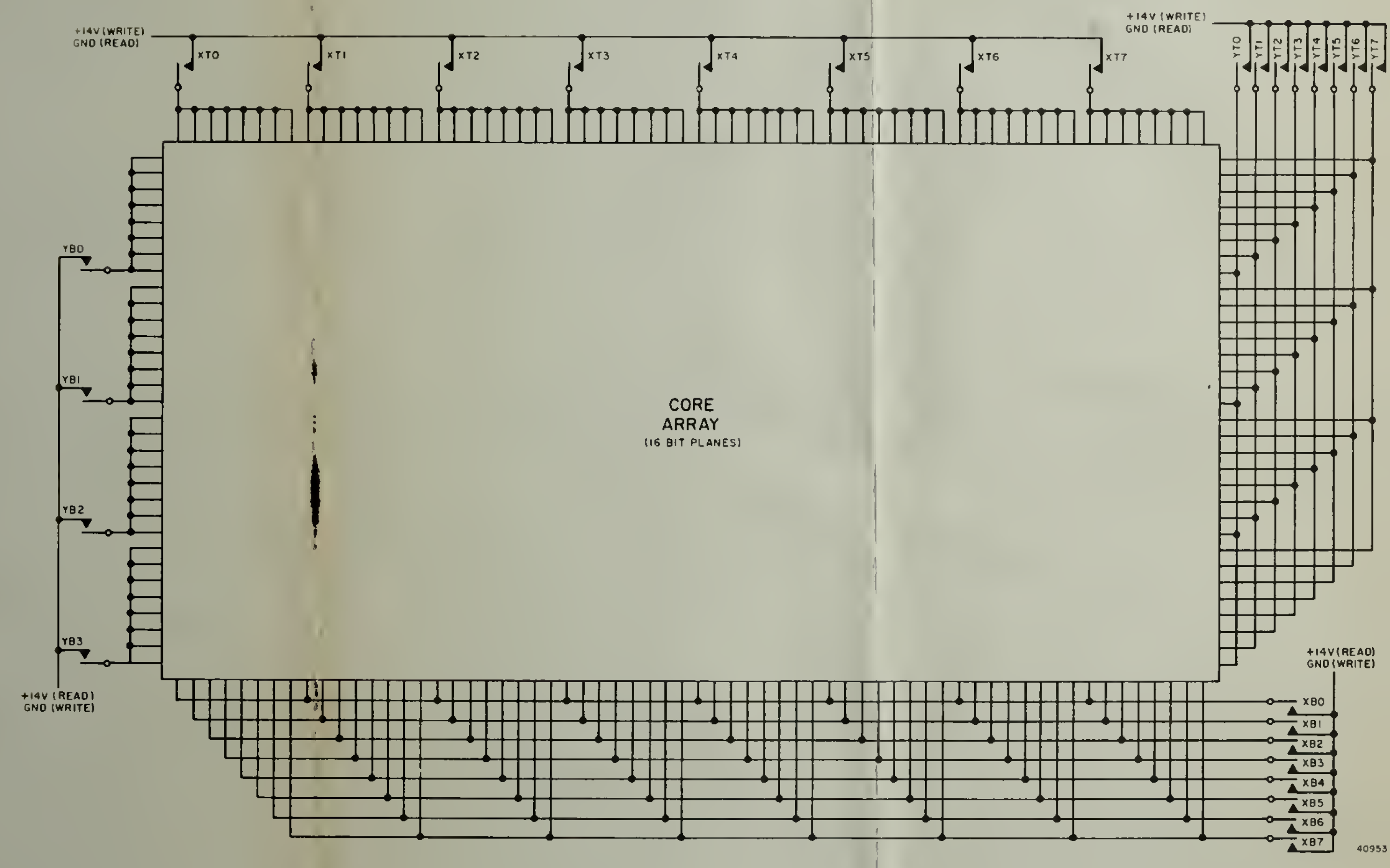

Figure 4-164. X and Y Selection, Simplified Diagram

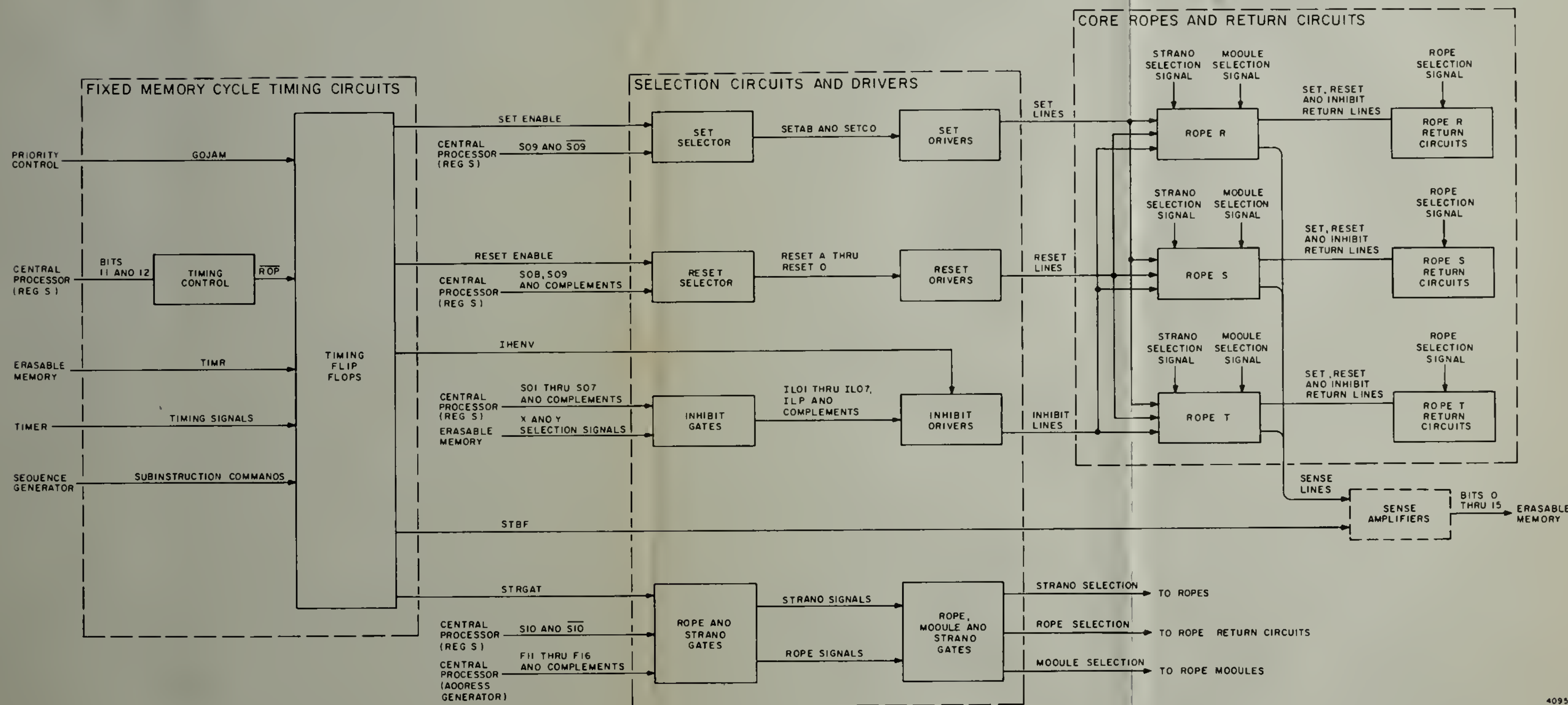

Figure 4-165. Fixed Memory, Functional Diagram

Table 4-LXXX. F Addressing

Register or Location Groups			Octal Address		FEXT	FBANK	S
			Pseudo	Real	7 6 5	16 14 13 12 11	12 11 10 9 8 7 6 5 4 3 2 1
FEXT-Channel X	Fixed F Memory	F-Bank 02	04000-05777	4000-5777 2000-3777	x x x x x x	x x x x x 0 0 0 1 0	1 0 y y y y y y y y y y 0 1 y y y y y y y y y y
		F-Bank 03	06000-07777	6000-7777 2000-3777	x x x x x x	x x x x x 0 0 0 1 1	1 1 y y y y y y y y y y 0 1 y y y y y y y y y y
	Variable F Memory	F-Bank 00	00000-01777	2000-3777	x x x	0 0 0 0 0	0 1 y y y y y y y y y y
		F-Bank 01	02000-03777	2000-3777	x x x	0 0 0 0 1	0 1 y y y y y y y y y y
		F-Bank 04	10000-11777	2000-3777	x x x	0 0 1 0 0	0 1 y y y y y y y y y y
		F-Bank 05	12000-13777	2000-3777	x x x	0 0 1 0 1	0 1 y y y y y y y y y y
		F-Bank 06	14000-15777	2000-3777	x x x	0 0 1 1 0	0 1 y y y y y y y y y y
		F-Bank 07	16000-17777	2000-3777	x x x	0 0 1 1 1	0 1 y y y y y y y y y y
		F-Bank 10	20000-21777	2000-3777	x x x	0 1 0 0 0	0 1 y y y y y y y y y y
		F-Bank 11	22000-23777	2000-3777	x x x	0 1 0 0 1	0 1 y y y y y y y y y y
		F-Bank 12	24000-25777	2000-3777	x x x	0 1 0 0 1	0 1 y y y y y y y y y y
		F-Bank 13	26000-27777	2000-3777	x x x	0 1 0 1 1	0 1 y y y y y y y y y y
		F-Bank 14	30000-31777	2000-3777	x x x	0 1 1 0 0	0 1 y y y y y y y y y y
		F-Bank 15	32000-33777	2000-3777	x x x	0 1 1 0 1	0 1 y y y y y y y y y y
		F-Bank 16	34000-35777	2000-3777	x x x	0 1 1 1 0	0 1 y y y y y y y y y y
		F-Bank 17	36000-37777	2000-3777	x x x	0 1 1 1 1	0 1 y y y y y y y y y y
		F-Bank 20	40000-41777	2000-3777	x x x	1 0 0 0 0	0 1 y y y y y y y y y y

⚠ x means 0 or 1 which does not have an effect on addressing.
y means 0 or 1 as defined by address.

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Table 4-LXXX. F Addressing

Register or Location Groups			Octal Address		FEXT	FBANK	S
			Pseudo	Real	7 6 5	16 14 13 12 11	12 11 10 9 8 7 6 5 4 3 2 1
FEXT-Channel X (cont)	Variable F Memory (cont)	F-Bank 21	42000-43777	2000-3777	x x x	1 0 0 0 1	0 1 y y y y y y y y y y
		F-Bank 22	44000-45777	2000-3777	x x x	1 0 0 1 0	0 1 y y y y y y y y y y
		F-Bank 23	46000-47777	2000-3777	x x x	1 0 0 1 1	0 1 y y y y y y y y y y
		F-Bank 24	50000-51777	2000-3777	x x x	1 0 1 0 0	0 1 y y y y y y y y y y
		F-Bank 25	52000-53777	2000-3777	x x x	1 0 1 0 1	0 1 y y y y y y y y y y
		F-Bank 26	54000-55777	2000-3777	x x x	1 0 1 1 0	0 1 y y y y y y y y y y
		F-Bank 27	56000-57777	2000-3777	x x x	1 0 1 1 1	0 1 y y y y y y y y y y
FEXT Channel 0-3		F-Bank 30	060000-061777	2000-3777	0 x x	1 1 0 0 0	0 1 y y y y y y y y y y
		F-Bank 31	062000-063777	2000-3777	0 x x	1 1 0 0 1	0 1 y y y y y y y y y y
		F-Bank 32	064000-065777	2000-3777	0 x x	1 1 0 1 0	0 1 y y y y y y y y y y
		F-Bank 33	066000-067777	2000-3777	0 x x	1 1 0 1 1	0 1 y y y y y y y y y y
		F-Bank 34	070000-071777	2000-3777	0 x x	1 1 1 0 0	0 1 y y y y y y y y y y
		F-Bank 35	072000-073777	2000-3777	0 x x	1 1 1 0 1	0 1 y y y y y y y y y y
		F-Bank 36	074000-075777	2000-3777	0 x x	1 1 1 1 0	0 1 y y y y y y y y y y
		F-Bank 37	076000-077777	2000-3777	0 x x	1 1 1 1 1	0 1 y y y y y y y y y y

△ x means 0 or 1 which does not have an effect on addressing.
y means 0 or 1 as defined by address.

(Sheet 2 of 4)

Table 4-LXXX. F Addressing

Register or Location Groups		Octal Address		FEXT	FBANK	S
		Pseudo	Real	7 6 5	16 14 13 12 11	12 11 10 9 8 7 6 5 4 3 2 1
FEXT-Channel 4	F-Bank 40	100000-101777	2000-3777	1 0 0	1 1 0 0 0	0 1 y y y y y y y y y y
	F-Bank 41	102000-103777	2000-3777	1 0 0	1 1 0 0 1	0 1 y y y y y y y y y y
	F-Bank 42	104000-105777	2000-3777	1 0 0	1 1 0 1 0	0 1 y y y y y y y y y y
	F-Bank 43	106000-107777	2000-3777	1 0 0	1 1 0 1 1	0 1 y y y y y y y y y y
	F-Bank 44	110000-111777	2000-3777	1 0 0	1 1 1 0 0	0 1 y y y y y y y y y y
	F-Bank 45	112000-113777	2000-3777	1 0 0	1 1 1 0 1	0 1 y y y y y y y y y y
	F-Bank 46	114000-115777	2000-3777	1 0 0	1 1 1 1 0	0 1 y y y y y y y y y y
FEXT-Channel 5	F-Bank 47	116000-117777	2000-3777	1 0 0	1 1 1 1 1	0 1 y y y y y y y y y y
	F-Bank 50	120000-121777	2000-3777	1 0 1	1 1 0 0 0	0 1 y y y y y y y y y y
	F-Bank 51	122000-123777	2000-3777	1 0 1	1 1 0 0 1	0 1 y y y y y y y y y y
	F-Bank 52	124000-125777	2000-3777	1 0 1	1 1 0 1 0	0 1 y y y y y y y y y y
	F-Bank 53	126000-127777	2000-3777	1 0 1	1 1 0 1 1	0 1 y y y y y y y y y y
	F-Bank 54	130000-131777	2000-3777	1 0 1	1 1 1 0 0	0 1 y y y y y y y y y y
	F-Bank 55	132000-133777	2000-3777	1 0 1	1 1 1 0 1	0 1 y y y y y y y y y y
	F-Bank 56	134000-135777	2000-3777	1 0 1	1 1 1 1 0	0 1 y y y y y y y y y y
	F-Bank 57	136000-137777	2000-3777	1 0 1	1 1 1 1 1	0 1 y y y y y y y y y y

△ x means 0 or 1 which does not have an effect on addressing.
y means 0 or 1 as defined by address.

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Table 4-LXXX. F Addressing

Register or Location Groups		Octal Address		FEXT	FBANK	S
		Pseudo	Real	7 6 5	16 14 13 12 11	12 11 10 9 8 7 6 5 4 3 2 1
FEXT-Channel 6	F-Bank 60	140000-141777	2000-3777	1 1 0	1 1 0 0 0	0 1 y y y y y y y y y y
	F-Bank 61	142000-143777	2000-3777	1 1 0	1 1 0 0 1	0 1 y y y y y y y y y y
	F-Bank 62	144000-145777	2000-3777	1 1 0	1 1 0 1 0	0 1 y y y y y y y y y y
	F-Bank 63	146000-147777	2000-3777	1 1 0	1 1 0 1 1	0 1 y y y y y y y y y y
	F-Bank 64	150000-151777	2000-3777	1 1 0	1 1 1 0 0	0 1 y y y y y y y y y y
	F-Bank 65	152000-153777	2000-3777	1 1 0	1 1 1 0 1	0 1 y y y y y y y y y y
	F-Bank 66	154000-155777	2000-3777	1 1 0	1 1 1 1 0	0 1 y y y y y y y y y y
	F-Bank 67	156000-157777	2000-3777	1 1 0	1 1 1 1 1	0 1 y y y y y y y y y y
FEXT-Channel 7	F-Bank 70	160000-161777	2000-3777	1 1 1	1 1 0 0 0	0 1 y y y y y y y y y y
	F-Bank 71	162000-163777	2000-3777	1 1 1	1 1 0 0 1	0 1 y y y y y y y y y y
	F-Bank 72	164000-165777	2000-3777	1 1 1	1 1 0 1 0	0 1 y y y y y y y y y y
	F-Bank 73	166000-167777	2000-3777	1 1 1	1 1 0 1 1	0 1 y y y y y y y y y y
	F-Bank 74	170000-171777	2000-3777	1 1 1	1 1 1 0 0	0 1 y y y y y y y y y y
	F-Bank 75	172000-173777	2000-3777	1 1 1	1 1 1 0 1	0 1 y y y y y y y y y y
	F-Bank 76	174000-175777	2000-3777	1 1 1	1 1 1 1 0	0 1 y y y y y y y y y y
	F-Bank 77	176000-177777	2000-3777	1 1 1	1 1 1 1 1	0 1 y y y y y y y y y y

△ x means 0 or 1 which does not have an effect on addressing.
y means 0 or 1 as defined by address.

(Sheet 4 of 4)

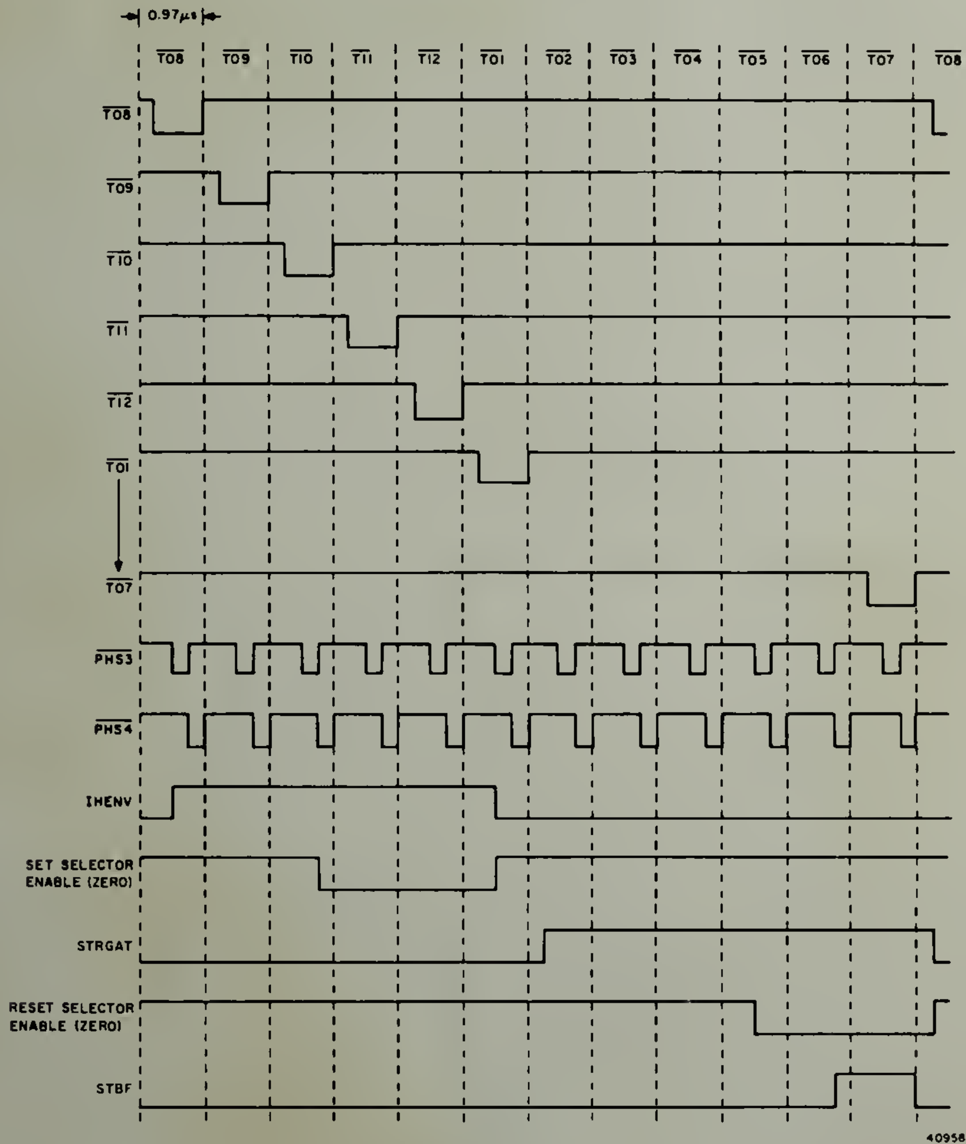

Figure 4-166. Fixed Memory, Timing Diagram

4-5.8.2.3 Core Ropes and Return Circuits. The drive lines (2 set, 4 reset, and 16 inhibit) threading the three ropes are connected in parallel, but return to three separate rope return circuits. Thus, a particular rope is selected by enabling the appropriate rope return circuit. This enabling occurs when one of three rope selection signals is received. At the same time, one of the two modules in a rope will be enabled by a module selection signal.

A strand consists of 16 sense lines (one per bit) and there are 12 strands per module for a total of 72 strands in fixed memory. However, only one strand select signal is present at a time. The 12 strands thread or bypass all cores in a module. Therefore, when a strand select signal is present, one word (one of twelve) of each core in a module is conditioned.

The combination of the inhibit, set, and reset lines are then used to select one core of the 512 cores in a module. During reset time the selected word is detected and amplified by 16 sense amplifiers which are enabled by signal STBF.

4-5.8.2.4 Sense Amplifiers. As in erasable memory, there are 16 sense amplifiers in fixed memory. Each amplifier amplifies the data on the selected sense line and forwards the data through the erasable memory sense amplifiers, when enabled by timing signal STBF.

4-5.9 POWER SUPPLY. Power required for operation of the LGC is provided by two mechanically identical and electrically interchangeable power supplies. Conversion is accomplished by tray wiring. The power supply (figure 4-167) consists of a +4 vdc power supply, +14 vdc power supply, and alarm detection circuits.

4-5.9.1 +4 VDC and +14 VDC Power Supplies Functional Description. The +4 vdc and +14 vdc power supplies each consist of a voltage regulator, power input and output circuits, and a standby switching circuit. The voltage outputs (+4 vdc and BPLUS) are determined by minor circuit changes and sync signals from the timer.

Primary power of +28 vdc (+28 DCB) from the LEM electrical power system is applied to the power input circuit of the +4 vdc power supply, filtered and applied to the power output circuit. A second filter supplies output +28 COM to the interface circuits of tray A, alarm detection circuits of tray B, and the DSKY. A zener diode regulator in the power input circuit is to supply 9.2 vdc to the voltage regulator. The voltage regulator is a parallel regulator which operates on a 50 kc sync signal from the timer ($\overline{\text{SYNC4}}$). $\overline{\text{SYNC4}}$ triggers a multivibrator circuit in the voltage regulator, the output of which is of sufficient duration to provide 4 vdc to the power output circuit. The 4 vdc output is regulated by feedback from the power output circuit to the voltage regulator. Input signal CNTRL 1 allows simulated failure of the power supply under control of the CTS during subsystem test. Standby operation, which is initiated by the STBY button on the DSKY, allows the LGC to conserve power by operating in a low power mode. Power supply output +4 SW is disabled during the standby mode of operation by signal $\overline{\text{SBYREL}}$.

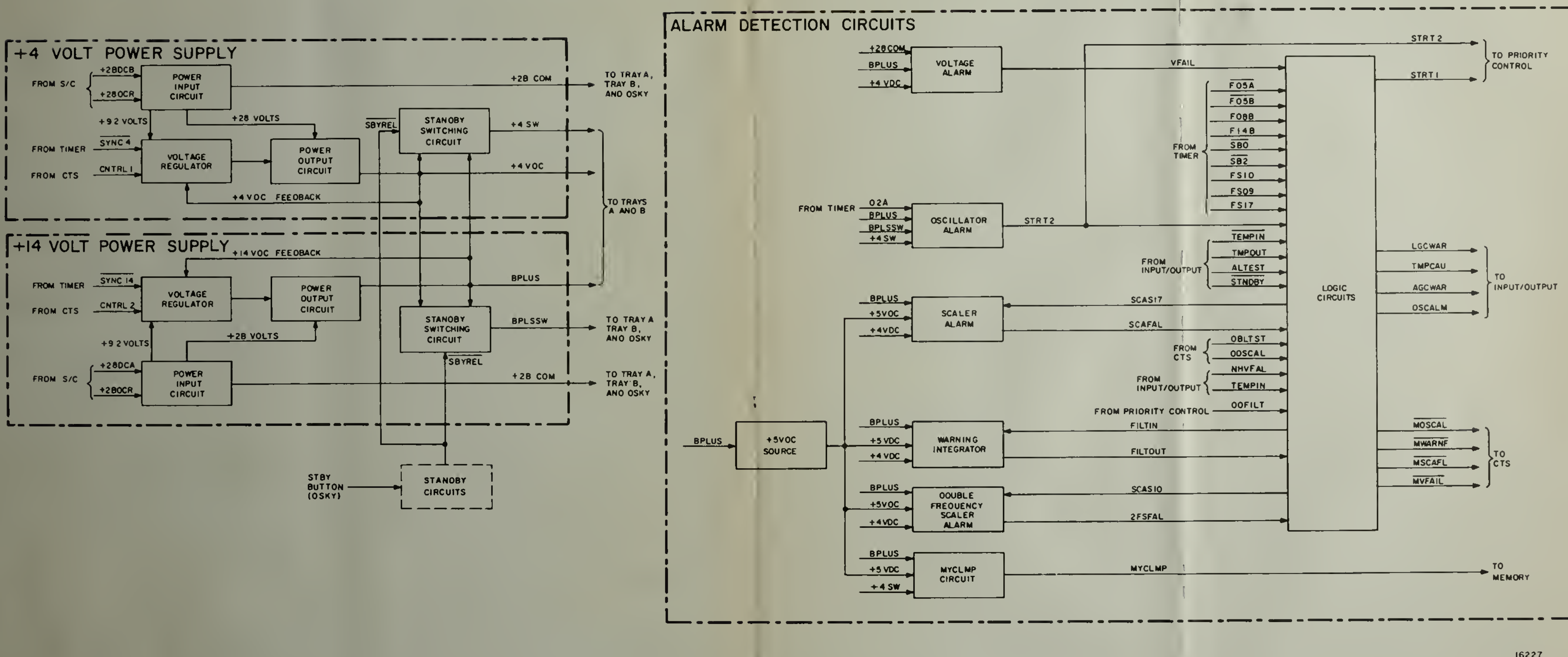

Figure 4-167. Power Supply Functional Diagram

Operation of the +14 volt power supply is identical to the +4 volt power supply with the exception that a 100 kc sync signal ($\overline{\text{SYNC 14}}$) is used instead of 50 kc and the power source is +28 DCA instead of +28 DCB. The +14 volt output is regulated by feedback of the BPLUS output to the voltage regulator. During standby operation power supply output BPLSSW is disabled by signal $\overline{\text{SBYREL}}$.

4-5.9.2 Alarm Detection Circuits Functional Description. The alarm detection circuits consist of voltage, oscillator, scaler, and double frequency scaler alarm circuits, a warning integrator, a memory clamp (MYCLMP) circuit, and associated logic circuits. These circuits are included at this time because their operation depends directly on the presence of outputs from the power supplies.

The voltage alarm circuit monitors the +28 COM, BPLUS, and +4 vdc outputs and generates a signal VFAIL for an out-of-limits condition or complete failure of any one of these power supply outputs. Signal VFAIL conditioned by timing signals $\overline{\text{F05A}}$ and $\overline{\text{F05B}}$, will generate signal STRT1 from the logic circuits, provided it is not inhibited by interface signal NHVFAL. Signal STRT1, when applied to priority control, causes a GOJAM condition. Simultaneously, if the computer is in the standby mode, an input to the warning integrator (FILTIN) is generated. This input is controlled by signal $\overline{\text{STNDBY}}$.

The oscillator alarm circuit generates signal STRT2 if the LGC oscillator (signal Q2A) should fail or the LGC is in the low power mode (STANDBY). A delay circuit in the oscillator alarm assures a GOJAM condition, via STRT2 to priority control, until the oscillator starts running during a powerup condition. STRT2 will also cause the generation of signal OSCALM from the logic circuits.

There are two scaler alarm circuits in the LGC; scaler alarm and double frequency scaler alarm. The scaler alarm circuit provides a check on scaler stage 17 (signal SCAS17 conditioned by signal FS17 from the timer) and generates signal SCAFAL should stage 17 fail to produce pulses. Signal SCAFAL generates signals AGCWAR and LGCWAR directly from the logic circuits. Signal DOSCAL from the CTS is used to test the operation of the scaler alarm via signal SCAS17. Double frequency scaler alarm generates signal 2FSFAL if the 100 pps scaler stage (signal SCAS10 from the logic circuits conditioned by signals FS09, and FS10 from the timer) should fail. Signal 2FSFAL provides an input to signal FILTIN which causes signals AGCWAR and LGCWAR to be generated from the logic circuits via signal FLTOUT. Signal DBLTST from the CTS is used to test the operation of the double frequency scaler alarm via signal SCAS10.

The warning integrator initiates the generation of warning signals AGCWAR and LGCWAR simultaneously from the logic circuits. Input signal FILTIN, conditioned by timing signals $\overline{\text{SB0}}$, $\overline{\text{SB2}}$, F08B, and F14B represents restart or counter fail signal (DOFILT), voltage fail in the standby mode, alarm test signal (ALTEST), or double frequency scaler alarm.

The MYCLMP circuit output inhibits access to memory should either power supply be out of its specified limits, fail completely, or be in the low power mode.

The incorporation of a +5 vdc source within the alarm detection circuits eliminates the need for more semiconductors and components normally used where a reference voltage is required such as in the scaler alarm, double frequency scaler alarm, warning integrator, and MYCLMP circuits.

4-5.9.3 +4 VDC Power Supply Detailed Description. The +4 vdc power supply (figure 4-168) consists of the power input, voltage regulator, power output, and standby switching circuits.

Primary power of +28 vdc B (WD168) from the spacecraft is applied through diode CR10 and indicator L3 to two filter networks and a regulator of the power input circuit. The first filter network (C19-22) supplies output +28 COM to the alarm detection circuits and DSKY. The second filter network (C8-C12, L2) supplies +28 vdc to the power output circuit. 28 vdc is routed through resistor R39, zener diode CR7, and emitter follower Q14 to supply 9.2 vdc for powering the voltage regulator circuit.

Transistor Q1 in the voltage regulator circuit is a differential amplifier which acts as a regulating device on the free running multivibrator circuit consisting of transistors Q6 and Q7. Zener diode CR1 and its associated circuitry establish a constant voltage reference at the base of Q1A. A portion of the +4 vdc output from the power supply is fed back to the base of Q1B. Resistor R13 is shunted by tray wiring to establish the reference level. Any difference between the reference voltage applied to the base of Q1A and the feedback voltage applied to the base of Q1B affects the pulse width output of the multivibrator, via transistor Q2, and opposes any change in the +4 vdc output. Input CNTRL 1, from the CTS, is applied to the base of Q1B and allows simulated failure of the +4 vdc power supply during subsystem test. Input W-910, from automatic checkout equipment (ACE), is applied to the base of Q1A and allows simulated failure of the +4 vdc power supply during LEM test. This signal may also be used during subsystem test by the CTS.

Input signal $\overline{\text{SYNC4}}$ (50 kc) is applied to the sync circuits (Q3, Q4, and Q5) and fixes the frequency of the output pulses from the free running multivibrator. The level of the +4 vdc regulator output, from Q8, is established by resistor R2 and by shunting out resistors R13, R20 and R30.

The regulator output pulses are applied to transistor power amplifier drivers Q9, Q10, and Q11 of the power output circuit. The output of these parallel transistors is fed through power amplifier Q12, filtered (C13-C15 and L1), and applied to output transistor Q13. Resistors R37 and R38 are connected in parallel by tray wiring for the +4 vdc power supply. The output of Q13 is the +4 vdc power supply output. The output of +4 vdc is also applied from charging network C16-C18 to the standby switching circuit.

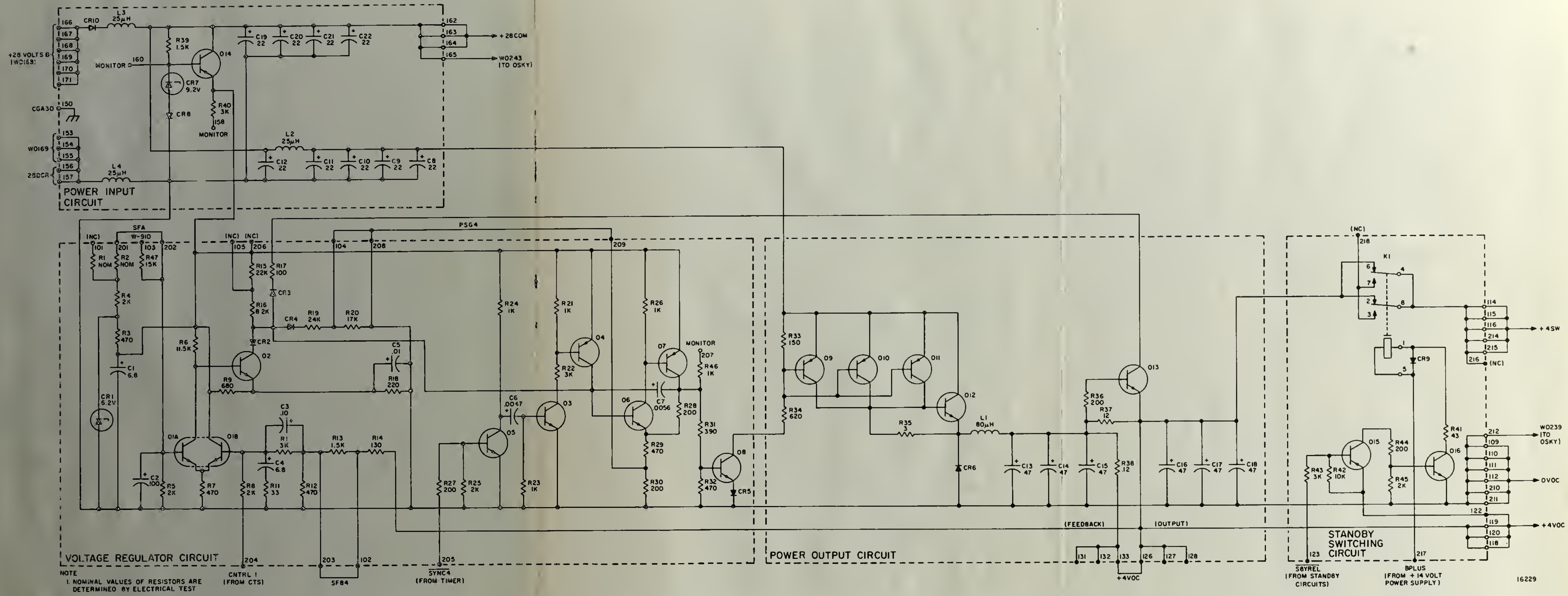

Figure 4-168. +4 VDC Power Supply, Schematic Diagram

Standby mode is controlled by the STBY pushbutton key on the DSKY and is used to conserve power. When the key is pressed, signal STBY is fed through the standby circuits to the standby switching circuit as signal $\overline{\text{SBYREL}}$. Signal $\overline{\text{SBYREL}}$ turns transistor Q15 on which turns transistor Q16 on, energizes K1 and disables output +4 SW. BPLUS used to energize the coil of K1 is supplied from the +14 volt power supply output. With output signal +4 SW disabled during the standby mode the only LGC circuits operating are the power supplies (outputs +4 vdc and BPLUS), oscillator, interface, and the scaler and clock divider circuits. This is necessary for keeping track of real time and supplying synchronization signals to other spacecraft systems.

Power distribution for tray A is shown in table 4-LXXXI. The distribution of power and filtering for tray B is illustrated and discussed individually later.

4-5.9.4 +14 VDC Power Supply Detailed Description. Operation of the +14 vdc power supply (figure 4-169) is identical to the +4 vdc power supply except that the level of the regulator circuit output is established by resistor R1 and by shunting out resistor R15. Inputs W-911 and CNTRL 2 allow simulated failure of the +14 vdc power supply during test, and input $\overline{\text{SYNC14}}$ (100 kc) fixes the frequency of the output pulses from the free running multivibrator. During the standby mode output BPLSSW is disabled.

4-5.9.5 Alarm Detection Circuits Detailed Description. The alarm detection circuits (figure 4-170) monitor the outputs of the power supply, oscillator, scaler, and priority control and generate a restart, failure, caution, or warning signal if any of the outputs should fail.

The voltage alarm circuit consists of a constant current source (Q1 and Q2), voltage divider (R11 thru R19), five differential amplifiers (Q3 thru Q7), and output transistors (Q8 thru Q10). The +28 COM input from both the +4 and +14 volt power supplies is applied to parallel transistors Q1 and Q2 where a constant current source is established. Zener diodes CR4 and CR5 in the collector circuit of Q2 supply +12.4 volts as a reference voltage to the voltage divider and differential amplifiers. Capacitor C1 acts as a storage device and is capable of powering the voltage alarm for a short period of time should the +28 volt supply fail abruptly or decay rapidly. The +28 COM input is also filtered by R3, R4, R5 and C4 and applied to detector Q7. Normally, Q7A is off, Q7B is on, and output transistor Q10 is off. If the +28 COM input should decrease below approximately +18 volts, Q7A will conduct, turn transistor Q10 on and generate output VFAIL. Similar operation occurs for the +4 and +14 volt detector circuits. BPLUS is divided and filtered (R1, R7, and C2) before being applied to detectors Q3 and Q4. Transistors Q3 and Q4 are the high and low limit detectors respectively for the +14 volt power supply. If the +14 volt power supply measures approximately +16 volts Q3A will conduct, turn on transistor Q8 and generate VFAIL. If the +14 volts decreases to approximately +12 volts Q4A will conduct, turn on transistor Q9 and generate VFAIL. +4 vdc is filtered by R2 and C3 before being applied to detectors Q5 and Q6. Transistors Q5 and Q6 are the high and low limit detectors respectively for the +4 volt power supply. If the +4 volt power supply increases to approximately +4.5 volts, transistor Q5A will conduct, turn on transistor Q8 and generate VFAIL. If the +4 volt input decreases to approximately 3.5 volts transistor Q6A will

conduct, turn on transistor Q9 and generate VFAIL. Signal VFAIL is applied to the voltage alarm circuit where it will generate signal STRT1, subject to timing signals $\overline{\text{F05A}}$ and $\overline{\text{F05B}}$ and if not inhibited by interface signal NHVFAL. Signal STRT1, when applied to priority control, causes signal GOJAM.

The oscillator alarm inputs are a 1.024 megacycle square wave (Q2A) from the timer and +14 volts (BPLSSW), +4 volts (+4SW) and BPLUS from the power supply. Normally, transistors Q12, Q16, and Q17 are off, Q13, Q14, and Q15 are on, and C7 is fully charged to +14 volts. If Q2A, +4SW, or BPLSSW is not present, Q12 is turned on and C7 discharges. Transistors Q13, Q14, and Q15 are off; transistors Q16 and Q17 are on generating signal STRT2. When the inputs are all present again it will take approximately 250 milliseconds for the complete circuit to be operable. This is accomplished by the time it takes to charge capacitor C7. The same situation occurs when the computer is initially turned on or when the computer is switched from standby to operate. Signal STRT2, when applied to priority control, causes signal GOJAM. Signal STRT2, when applied to the oscillator alarm logic circuit in module A13, causes signal OSCALM to be generated and applied to input-output. Signal CCH33 from input-output is a clear signal for flip-flop 41232-41233.

The +5 vdc voltage source provides a reference voltage to the detector circuits in the scaler alarm, double frequency scaler alarm, warning integrator, and MYCLMP circuits.

The scaler alarm circuit receives input FS17 (0.78125 pps) from the timer and produces signal SCAS17 from logic gate 32258. Signal DOSCAL, from the CTS, is used for testing the scaler alarm circuit. Normally transistors Q18, Q19, and Q20 are off. The voltage present in parallel capacitors C9 and C13 is less than the turnon voltage required for Q22; therefore, transistors Q21, Q22, and Q23 are off and signal SCAFAL is approximately 0 vdc. If the scaler should fail, transistor Q18 is turned on, the signal at its collector is differentiated by C8 and R70 and fed to Q20. Transistor Q20 is turned on, which turns Q19 on and supplies the base drive required to keep Q20 on. Transistor Q21 is on and supplies the drive necessary to turn Q22 on. Reference voltage (+5 VDC) is supplied through CR6 and Q22, and applied to Q21 and Q23 where it clamps Q21 on, turns Q23 on and generates signal SCAFAL to a logic circuit which in turn will generate a warning signal to the DSKY and input-output.

The double frequency scaler alarm monitors signal SCAS10 (100 pps) from its logic circuit in module A3. However, signal SCAS10 is not equal in duty cycle to FS10. Signal SCAS10 has a 25% duty cycle generated as a result of combining signals FS09 and FS10 from the timer. Signal CON 2 from module A3 is applied to warning filter module A13 where, when combined with signal FS10, will generate signal CON 3. Thus, signal SCAS10 is equal to signal CON 3. Signal DBLTST, from the CTS, is used for testing the double frequency scaler alarm circuit. Transistors Q35, Q37, and Q38 are normally on and Q36 is normally off. When transistor Q34 is on a negative going transition will be coupled through capacitor C14. This transition will be routed through Q37 and Q38. The pulse width of this change is determined by time constant C14 and R119. The output of Q38 is supplied as signal 2FSFAL to the warning filter

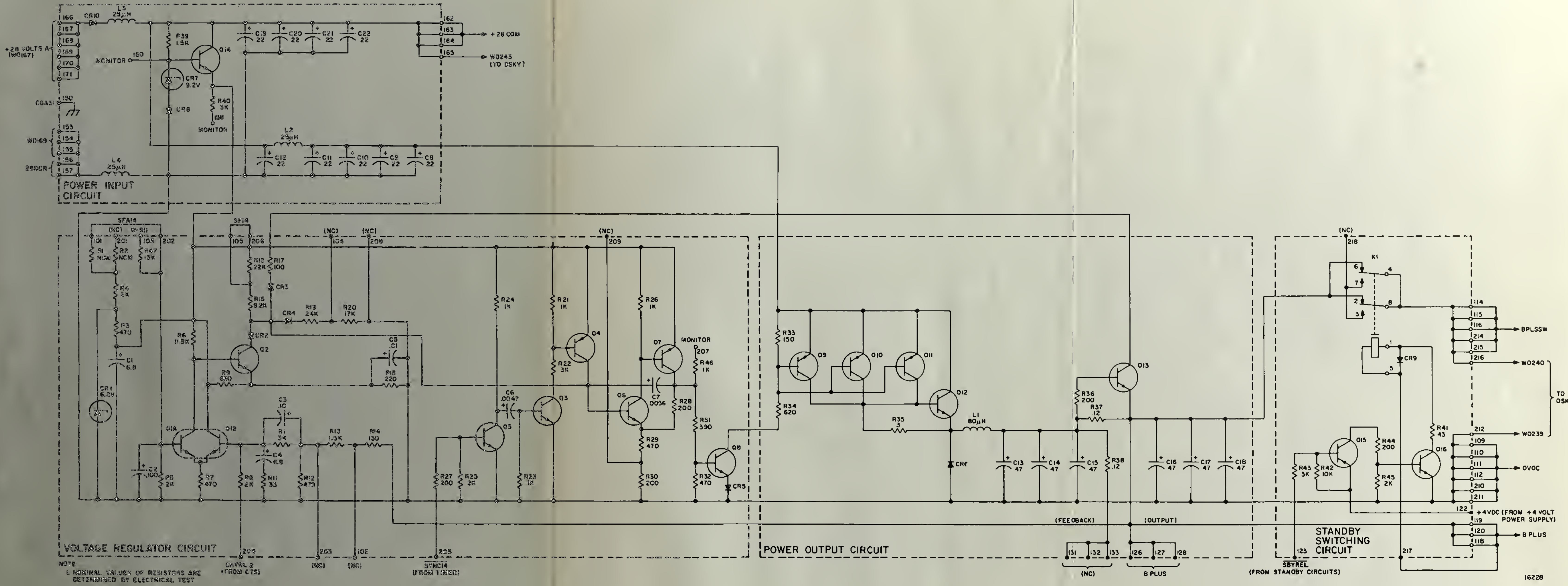

Figure 4-169. +14 VDC Power Supply, Schematic Diagram

where it is compared with signal CON 3 at the input of gate 41243. Normally gate 41243 yields a ZERO as its output. However, if signal SCAS10 increases to approximately 200 pps, the output will be a series of ONE's.

The MYCLMP circuit operates identical to that of a voltage alarm circuit. The differential amplifier Q24 has reference voltage (+5 vdc) applied to one side (Q23B) and +4SW applied to the other side (Q24A). Normally transistor Q25 is off and output signal MYCLMP is approximately 0 vdc. If the +4 volt power supply should fail or the computer is put into the standby mode, the +4SW is decreased to 0 vdc and Q24A cuts off. Q24B then conducts causing Q25 to turn on and generate signal MYCLMP to memory where it inhibits any access to the memory circuits.

The warning filter performs logic gating for the following inputs:

(1) $\overline{\text{VFAIL}}$ and $\overline{\text{STNDBY}}$.

(2) 2FSFAL.

(3) DOFILT.

(4) ALTEST.

Any one of the above conditions sets flip-flop 41211-41212. The flip-flop output is applied through gate 41213 and in turn sets flip-flop 41214-41215, subject to timing signals $\overline{\text{SB0}}$ and $\overline{\text{F14B}}$. The output of flip-flop 41214-41215, FILTIN, is applied to the warning integrator. All occurrences of these input conditions are stretched so that no more than one input to the warning integrator is generated in each 160 millisecond period. This is controlled by timing signal F14B. Thus, the output signal FILTIN has a maximum rate of 6 pps.

Each of the pulse inputs to the warning integrator has a duration of 1.125 milliseconds, and because of this the warning integrator will not receive an input pulse each time a restart is called for by the computer. Normally transistors Q28 through Q33, with the exception of Q30B, are off. A positive pulse turns on transistor Q28 which will turn on constant current source Q29 and supply a charge to capacitor C12. This charge will add a voltage step to C12. When five successive pulses are received it will cause the voltage on C12 to overcome the threshold voltage (approximately +4 volts) of Q30A. Turning Q30A on will turn Q21, Q32, and Q33 on which will make the detector regenerative. Signal FLTOUT will remain high as an output as long as pulses are forthcoming. However, if only the above occurs it would take approximately five seconds for C12 to discharge through R100. Thus, signal FLTOUT is present for approximately 5 seconds.

Signal FLTOUT from the warning integrator and signal SCAFAL from the scaler alarm are applied to gates 41222 through 41224 and flip-flop 41225-41226 where, if either or both is high, signals $\overline{\text{MSCAFL}}$, $\overline{\text{MWARNF}}$, LGCWAR, and AGCWAR will be generated. Signal CCH33 is a clear signal for flip-flop 41225-41226.

Table 4-LXXXI. Power Distribution

Module	Voltage	Pins	Distribution
A1	0VDC	112, 136, 160	To pin 5 and unused inputs 38100 series gates
	0VDC	212, 236, 260	To pin 5 and unused inputs 38200 series gates
	0VDC	312, 336, 360	To pin 5 and unused inputs 38300 series gates
	0VDC	412, 436, 460	To pin 5 and unused inputs 38400 series gates
	+4VDC	122, 150	To pin 10 of 38100 series gates
	+4VDC	222, 250	To pin 10 of 38200 series gates
	+4VDC	322, 350	To pin 10 of 38300 series gates
	+4VDC	422, 450	To pin 0 of 38400 series gates
A2	0VDC	112, 136, 160	To pin 5 and unused inputs of 37100 series gates
	0VDC	212, 236, 260	To pin 5 and unused inputs of 37200 series gates
	0VDC	312, 336, 360	To pin 5 and unused inputs of 37300 series gates
	0VDC	412, 436, 460	To pin 5 and unused inputs of 37400 series gates
	+4VDC	122, 150	To pin 10 of 37100 series gates
	+4VDC	222, 250	To pin 10 of 37200 series gates

(Sheet 1 of 14)

Table 4-LXXXI. Power Distribution

Module	Voltage	Pins	Distribution
A2	+4SW	324,348	To pin 10 of 37300 series gates
	+4SW	424,448	To pin 10 of 37400 series gates
A3	0VDC	112,136,160	To pin 5 and unused inputs of 30000 series gates
	0VDC	212,236,260	To pin 5 and unused inputs of 30100 series gates
	0VDC	312,336,360	To pin 5 and unused inputs of 30300 series gates
	0VDC	412,436,460	To pin 5 and unused inputs of 30400 series gates
	+4SW	124,148	To pin 10 of 30000 series gates
	+4SW	224,248	To pin 10 of 30100 series gates
	+4SW	324,348	To pin 10 of 30300 series gates
	+4SW	424,448	To pin 10 of 30400 series gates
A4	0VDC	112,136,160	To pin 5 and unused inputs of 36100 series gates
	0VDC	212,236,260	To pin 5 and unused inputs of 36200 series gates
	0VDC	312,336,360	To pin 5 and unused inputs of 36300 series gates
	0VDC	412,436,460	To pin 5 and unused inputs of 36400 series gates

(Sheet 2 of 14)

Table 4-LXXXI. Power Distribution

Module	Voltage	Pins	Distribution
A4	+4SW	124,148	To pin 10 of 36100 series gates
	+4SW	224,248	To pin 10 of 36200 series gates
	+4SW	324,348	To pin 10 of 36300 series gates
	+4SW	424,448	To pin 10 of 36400 series gates
A5	0VDC	112,136,160	To pin 5 and unused inputs of 39100 series gates
	0VDC	212,236,260	To pin 5 and unused inputs of 39200 series gates
	0VDC	312,336,360	To pin 5 and unused inputs of 39300 series gates
	0VDC	412,436,460	To pin 5 and unused inputs of 39400 series gates
	+4SW	124,148	To pin 10 of 39100 series gates
	+4SW	224,248	To pin 10 of 39200 series gates
	+4SW	324,348	To pin 10 of 39300 series gates
	+4SW	424,448	To pin 10 of 39400 series gates
A6	0VDC	112,136,160	To pin 5 and unused inputs of 40100 series gates
	0VDC	212,236,260	To pin 5 and unused inputs of 40200 series gates

(Sheet 3 of 14)

Table 4-LXXXI. Power Distribution

Module	Voltage	Pins	Distribution
A6	0VDC	312,336,360	To pin 5 and unused inputs of 40300 series gates
	0VDC	412,436,460	To pin 5 and unused inputs of 40400 series gates
	+4SW	124,148	To pin 10 of 40100 series gates
	+4SW	224,248	To pin 10 of 40200 series gates
	+4SW	324,348	To pin 10 of 40300 series gates
	+4SW	424,448	To pin 10 of 40400 series gates
A7	0VDC	112,136,160	To pin 5 and unused inputs of 33100 series gates
	0VDC	212,236,260	To pin 5 and unused inputs of 33200 series gates
	0VDC	312,336,360	To pin 5 and unused inputs of 33300 series gates
	0VDC	412,436,460	To pin 5 and unused inputs of 33400 series gates
	+4SW	124,148	To pin 10 of 33100 series gates
	+4SW	224,248	To pin 10 of 33200 series gates
	+4SW	324,348	To pin 10 of 33300 series gates
	+4SW	424,448	To pin 10 of 33400 series gates

(Sheet 4 of 14)

Table 4-LXXXI. Power Distribution

Module	Voltage	Pins	Distribution
A8	0VDC	112,136,160	To pin 5 and unused inputs of 51100 series gates
	0VDC	212,236,260	To pin 5 and unused inputs of 51200 series gates
	0VDC	312,336,360	To pin 5 and unused inputs of 51300 series gates
	0VDC	412,436,460	To pin 5 and unused inputs of 51400 series gates
	+4SW	124,148	To pin 10 of 51100 series gates
	+4SW	224,248	To pin 10 of 51200 series gates
	+4SW	324,348	To pin 10 of 51300 series gates
	+4SW	424,448	To pin 10 of 51400 series gates
A9	0VDC	112,136,160	To pin 5 and unused inputs of 52100 series gates
	0VDC	212,236,260	To pin 5 and unused inputs of 52200 series gates
	0VDC	312,336,360	To pin 5 and unused inputs of 52300 series gates
	0VDC	412,436,460	To pin 5 and unused inputs of 52400 series gates
	+4SW	124,148	To pin 10 of 52100 series gates
	+4SW	224,248	To pin 10 of 52200 series gates
	+4SW	324,348	To pin 10 of 52300 series gates

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Table 4-LXXXI. Power Distribution

Module	Voltage	Pins	Distribution
A9	+4SW	424,448	To pin 10 of 52400 series gates
A10	0VDC	112,136,160	To pin 5 and unused inputs of 53100 series gates
	0VDC	212,236,260	To pin 5 and unused inputs of 53200 series gates
	0VDC	312,336,360	To pin 5 and unused inputs of 53300 series gates
	0VDC	412,436,460	To pin 5 and unused inputs of 53400 series gates
	+4SW	124,148	To pin 10 of 53100 series gates
	+4SW	224,248	To pin 10 of 53200 series gates
	+4SW	324,348	To pin 10 of 53300 series gates
	+4SW	424,448	To pin 10 of 53400 series gates
A11	0VDC	112,136,160	To pin 5 and unused inputs of 54100 series gates
	0VDC	212,236,260	To pin 5 and unused inputs of 54200 series gates
	0VDC	312,336,360	To pin 5 and unused inputs of 54300 series gates
	0VDC	412,436,460	To pin 5 and unused inputs of 54400 series gates
	+4SW	124,148	To pin 10 of 54100 series gates
	+4SW	224,248	To pin 10 of 54200 series gates

(Sheet 6 of 14)

Table 4-LXXXI. Power Distribution

Module	Voltage	Pins	Distribution
A11	+4SW	324,348	To pin 10 of 54300 series gates
	+4SW	425,448	To pin 10 of 54400 series gates
A12	0VDC	112,136,160	To pin 5 and unused inputs of 34100 series gates
	0VDC	212,236,260	To pin 5 and unused inputs of 34200 series gates
	0VDC	312,336,360	To pin 5 and unused inputs of 34300 series gates
	0VDC	412,436,460	To pin 5 and unused inputs of 34400 series gates
	+4SW	124,148	To pin 10 of 34100 series gates
	+4SW	224,248	To pin 10 of 34200 series gates
	+4SW	324,348	To pin 10 of 34300 series gates
	+4SW	424,448	To pin 10 of 34400 series gates
A13	0VDC	112,136,160	To pin 5 and unused inputs of 41100 series gates
	0VDC	212,236,260	To pin 5 and unused inputs of 41200 series gates
	+4VDC	222,250	To pin 10 of 41200 series gates
	+4SW	124,128	To pin 10 of 41100 series gates

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Table 4-LXXXI. Power Distribution

Module	Voltage	Pins	Distribution
A14	0VDC	112, 136, 160	To pin 5 and unused inputs of 42100 series gates
	0VDC	212, 236, 260	To pin 5 and unused inputs of 42200 series gates
	0VDC	312, 336, 360	To pin 5 and unused inputs of 42300 series gates
	0VDC	412, 436, 460	To pin 5 and unused inputs of 42400 series gates
	+4SW	124, 148	To pin 10 of 42100 series gates
	+4SW	224, 248	To pin 10 of 42200 series gates
	+4SW	324, 348	To pin 10 of 42300 series gates
	+4SW	424, 448	To pin 10 of 42400 series gates
A15	0VDC	112, 136, 160	To pin 5 and unused inputs of 35100 series gates
	0VDC	212, 236, 260	To pin 5 and unused inputs of 35200 series gates
	0VDC	312, 336, 360	To pin 5 and unused inputs of 35300 series gates
	0VDC	412, 436, 460	To pin 5 and unused inputs of 35400 series gates
	+4SW	124, 148	To pin 10 of 35100 series gates
	+4SW	224, 248	To pin 10 of 35200 series gates

(Sheet 8 of 14)

Table 4-LXXXI. Power Distribution

Module	Voltage	Pins	Distribution
A15	+4SW	324,348	To pin 10 of 35300 series gates
	+4SW	424,448	To pin 10 of 35400 series gates
A16	0VDC	112,136,160	To pin 5 and unused inputs of 43100 series gates
	0VDC	212,236,260	To pin 5 and unused inputs of 43200 series gates
	0VDC	312,336,360	To pin 5 and unused inputs of 43300 series gates
	0VDC	412,436,460	To pin 5 and unused inputs of 43400 series gates
	+4SW	124,148	To pin 10 of 43100 series gates
	+4SW	224,248	To pin 10 of 43200 series gates
	+4SW	324,348	To pin 10 of 43300 series gates
	+4SW	424,448	To pin 10 of 43400 series gates
A17	0VDC	112,136,160	To pin 5 and unused inputs of 44100 series gates
	0VDC	212,236,260	To pin 5 and unused inputs of 44200 series gates
	0VDC	312,336,360	To pin 5 and unused inputs of 44300 series gates
	0VDC	412,436,460	To pin 5 and unused inputs of 44400 series gates

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Table 4-LXXXI. Power Distribution

Module	Voltage	Pins	Distribution
A17	+4SW	124,148	To pin 10 of 44100 series gates
	+4SW	224,248	To pin 10 of 44200 series gates
	+4SW	324,348	To pin 10 of 44300 series gates
	+4SW	424,448	To pin 10 of 44400 series gates
A18	0VDC	112,136,160	To pin 5 and unused inputs of 45100 series gates
	0VDC	212,236,260	To pin 5 and unused inputs of 45200 series gates
	0VDC	312,336,360	To pin 5 and unused inputs of 45300 series gates
	0VDC	412,436,460	To pin 5 and unused inputs of 45400 series gates
	+4VDC	150	To pin 10 of gates 45137 through 45159
	+4VDC	250	To pin 10 of gates 45261 and 45262
	+4SW	124	To pin 10 of gates 45101 through 45136
	+4SW	224,248	To pin 10 of 45200 series gates
	+4SW	324,348	To pin 10 of 45300 series gates
	+4SW	424,448	To pin 10 of 45400 series gates

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Table 4-LXXXI. Power Distribution

Module	Voltage	Pins	Distribution
A19	0VDC	112, 136, 160	To pin 5 and unused inputs of 46100 series gates
	0VDC	212, 236, 260	To pin 5 and unused inputs of 46200 series gates
	0VDC	312, 336, 360	To pin 5 and unused inputs of 46300 series gates
	0VDC	412, 436, 460	To pin 5 and unused inputs of 46400 series gates
	+4SW	124, 148	To pin 10 of 46100 series gates
	+ 4SW	224, 248	To pin 10 of 46200 series gates
	+4SW	324, 348	To pin 10 of 46300 series gates
	+4SW	424, 448	To pin 10 of 46400 series gates
A20	0VDC	112, 136, 160	To pin 5 and unused inputs of 31100 series gates
	0VDC	212, 236, 260	To pin 5 and unused inputs of 31200 series gates
	0VDC	312, 336, 360	To pin 5 and unused inputs of 31300 series gates
	0VDC	412, 436, 460	To pin 5 and unused inputs of 31400 series gates
	+4SW	124, 148	To pin 10 of 31100 series gates
	+4SW	224, 248	To pin 10 of 31200 series gates

(Sheet 11 of 14)

Table 4-LXXXI. Power Distribution

Module	Voltage	Pins	Distribution
A20	+4SW	324,348	To pin 10 of 31300 series gates
	+4SW	424,448	To pin 10 of 31400 series gates
A21	0VDC	112,136,160	To pin 5 and unused inputs of 32000 series gates
	0VDC	212,236,260	To pin 5 and unused inputs of 32200 series gates
	0VDC	312,336,360	To pin 5 and unused inputs of 32600 series gates
	0VDC	412,436,460	To pin 5 and unused inputs of 32500 series gates
	+4SW	124,148	To pin 10 of 32000 series gates
	+4SW	224,248	To pin 10 of 32200 series gates
	+4SW	324,348	To pin 10 of 32600 series gates
	+4SW	424,448	To pin 10 of 32500 series gates
A22	0VDC	112,136,160	To pin 5 and unused inputs of 47100 series gates
	0VDC	212,236,260	To pin 5 and unused inputs of 47200 series gates
	0VDC	312,336,360	To pin 5 and unused inputs of 47300 series gates
	0VDC	412,436,460	To pin 5 and unused inputs of 47400 series gates

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Table 4-LXXXI. Power Distribution

Module	Voltage	Pins	Distribution
A22	+4VDC	222	To pin 10 of gates 47227 and 47256
	+4SW	124,148	To pin 10 of 47100 series gates
	+4SW	224,248	To pin 10 of 47200 series gates, except gates 47227 and 47256
	+4SW	324,348	To pin 10 of 47300 series gates
	+4SW	424,448	To pin 10 of 47400 series gates
A23	0VDC	112,136,160	To pin 5 and unused inputs of 48100 series gates
	0VDC	212,236,260	To pin 5 and unused inputs of 48200 series gates
	0VDC	312,336,360	To pin 5 and unused inputs of 48300 series gates
	0VDC	412,436,460	To pin 5 and unused inputs of 48400 series gates
	+4SW	124,148	To pin 10 of 48100 series gates
	+4SW	224,248	To pin 10 of 48200 series gates
	+4SW	324,348	To pin 10 of 48300 series gates
	+4SW	424,448	To pin 10 of 48400 series gates

(Sheet 13 of 14)

Table 4-LXXXI. Power Distribution

Module	Voltage	Pins	Distribution
A24	0VDC	112, 136, 160	To pin 5 and unused inputs of 49100 series gates
	0VDC	212, 236, 260	To pin 5 and unused inputs of 49200 series gates
	0VDC	312, 336, 360	To pin 5 and unused inputs of 49300 series gates
	0VDC	412, 436, 460	To pin 5 and unused inputs of 49400 series gates
	+4VDC	222, 250	To pin 10 of gates 49201 through 49234 and gate 49255
	+4SW	124, 148	To pin 10 of 49100 series gates
	+4SW	224, 248	To pin 10 of gates 49235 through 49254
	+4SW	324, 348	To pin 10 of 49300 series gates
	+4SW	424, 448	To pin 10 of 49400 series gates

(Sheet 14 of 14)

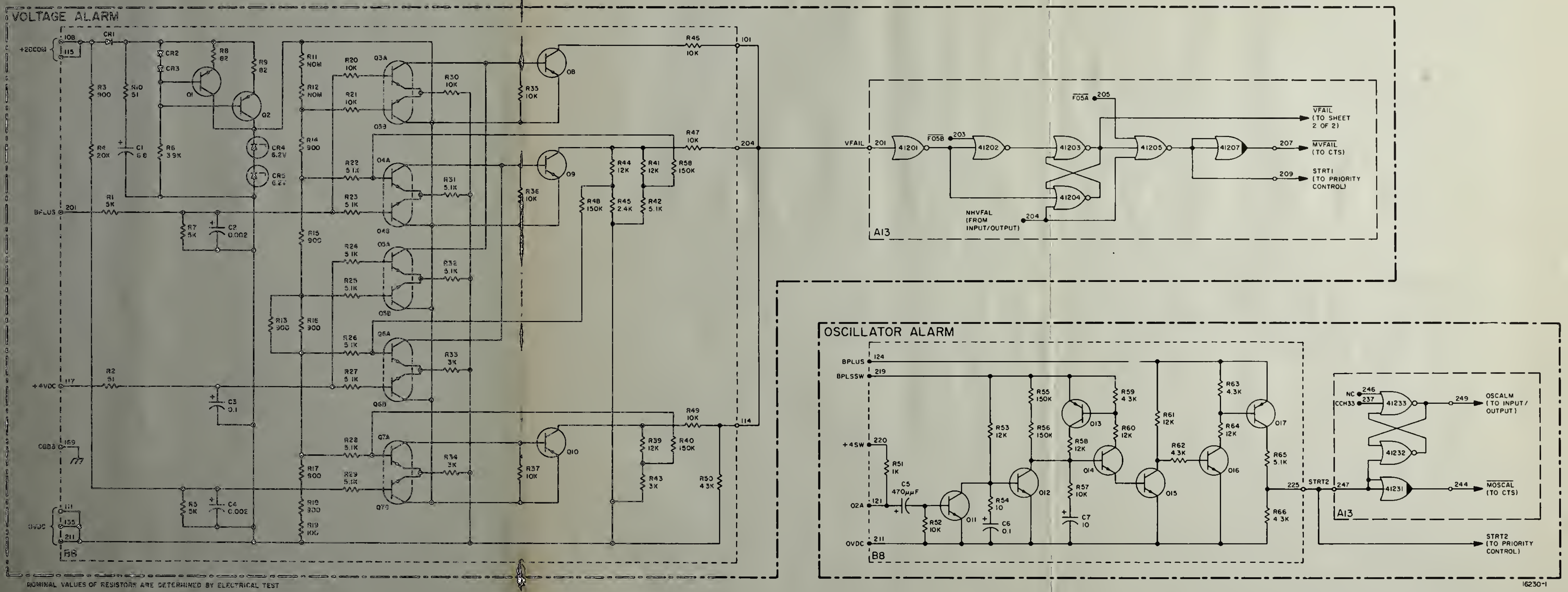

Figure 4-170. Alarm Detection Circuits, Schematic Diagram (Sheet 1 of 2)

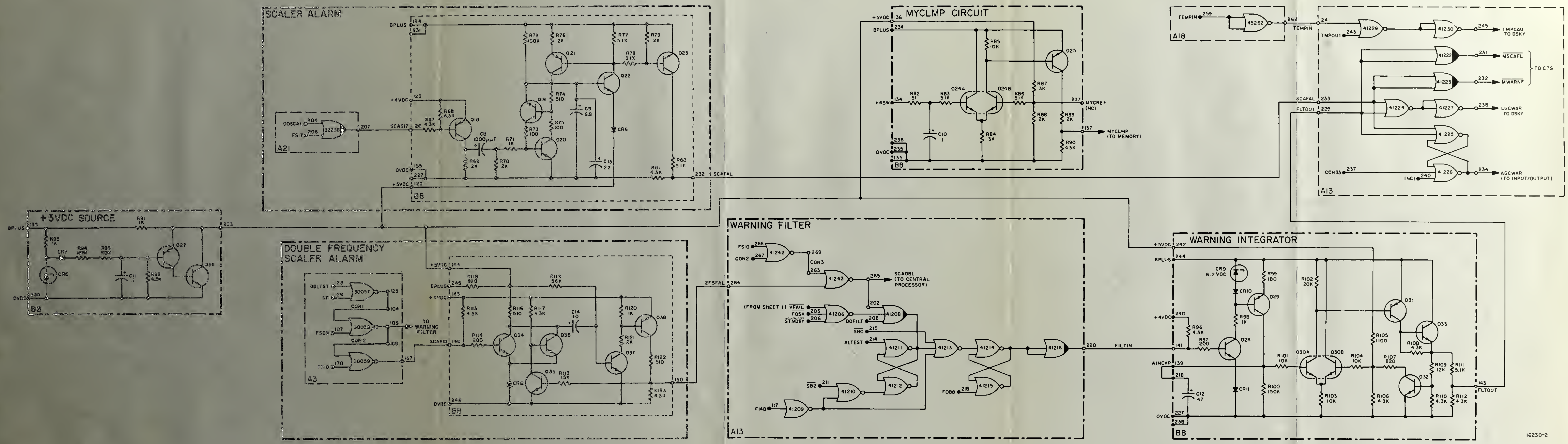

Figure 4-170. Alarm Detection Circuits, Schematic Diagram (Sheet 2 of 2)

If the IMU stable member temperature exceeds its design limits signal TEMPIN conditioned by signal TMPOUT will generate signal TMPCAU.

All LGC alarms are inhibited during the standby mode with the exception of AGCWAR and LGCWAR, which can be caused by a voltage fail or scaler fail, and TMPCAU, which is caused by an IMU temperature alarm.

4-5.10 DISPLAY AND KEYBOARD. The DSKY provides a means of communicating with the LGC. The DSKY allows the astronauts to load information into the LGC, request information from the LGC, initiate various programs stored in memory, and perform tests on the LGC and other subsystems of the PGNCS system. The DSKY also provides an indication of status and caution changes which may occur within the LGC, PGNCS, or other spacecraft systems.

4-5.10.1 DSKY Functional Description. The DSKY (figure 4-171) consists of a keyboard, power supply, decoder, relay matrix, status and caution circuits, and displays.

The keyboard contains the key controls with which the astronaut operates the DSKY. Each of the key controls is lighted by 115 vac, 400 cps. Inputs to the LGC initiated from the keyboard are processed by the program. The results are supplied to either the decoder and relay matrix or to the status and caution circuits for display. Each key when depressed, with the exception of standby, will produce a 5 bit code. The keycode enters into the LGC and initiates an interrupt to allow the data to be accepted. The key reset signal (+28 vdc) is generated each time a key is released, and conditions the LGC to accept another keycode. The reset code and signal (+28 vdc) is used when the astronaut wishes certain display indicators to go out. It also checks on whether a particular indicator is transient or permanent. The clear code is used when the astronaut wishes to clear displayed sign and digit information. Key release turns the control of displaying information on the DSKY over to the LGC. The standby signal (+28 vdc) initiates putting the LGC into the standby mode. It also initiates putting the LGC into operate mode when pressed a second time.

The power supply utilizes +28 vdc and +14 vdc from the LGC power supply and an 800 cps sync signal from the timer to generate a 250 volt, 800 cps display voltage. The display voltage is applied to the displays through the relay matrix and status and caution circuits.

The decoder receives a four bit relay word (bits 12 through 15) from channel 10 in the LGC. The decoded relay word, in conjunction with relay bits 1 through 11 from channel 10, energizes specific relays in the matrix. The relays are energized by the coincidence of a selection signal from the diode matrix in the decoder which produces a row selection signal, and relay bits which produce column selection signals. Relay selection allows the display voltage (250 vac) from the power supply to be routed to the proper sign and digit indicators. Relay selection also allows the alarm common (0 vdc) or +5 vdc from the PGNCS system, or from the LEM, to be routed through the relay to the PGNCS system or to the LEM (caution signals) or to the proper status and caution indicators respectively. The PGNCS caution signals from the relay matrix,

represented by 0 vdc, are PROG CAUTION, TRACKER, and GIMBAL LOCK. The status and caution indicators, lit by the +5 vdc are: PROG, TRACKER, GIMBAL LOCK, and NO ATT. All relays associated with the relay matrix are the latching type.

The status and caution circuits receive all LGC status and caution signals. Each signal is applied to a driver circuit and to an associated relay. When a relay is energized, it allows the voltage from the DSKY power supply (250 vac), or +5 vdc or 0 vdc from the PGNCS or LEM to be routed to the proper display indicators or equipment. The voltage from the power supply is routed through a relay to the computer activity indicator (COMP ACTY). The +5 vdc is routed through relays to the following status and caution indicators: UPLINK ACTY, RESTART, OPR ERR, KEY REL, and TEMP. The status and caution signals, represented by 0 vdc or an open circuit, are ISS WARNING, STBY, LGCWAR, TEMP CAUTION, and RESTART. All relays associated with the status and caution circuits are the non-latching type.

The displays consist of sign and digital (operational and data display) and status and caution indicators. The sign and digital indicators allow the astronaut to observe the data entered or requested from the keyboard. The status and caution indicators present an indication of any variance from certain normal operations.

4-6 SIGNAL CONDITIONER

This paragraph will supply detailed theory of operation for the signal conditioner when the information becomes available.

4-7 LEM OPTICAL RENDEZVOUS SUBSYSTEM

This paragraph will supply detailed theory of operation for the LORS when the information becomes available.

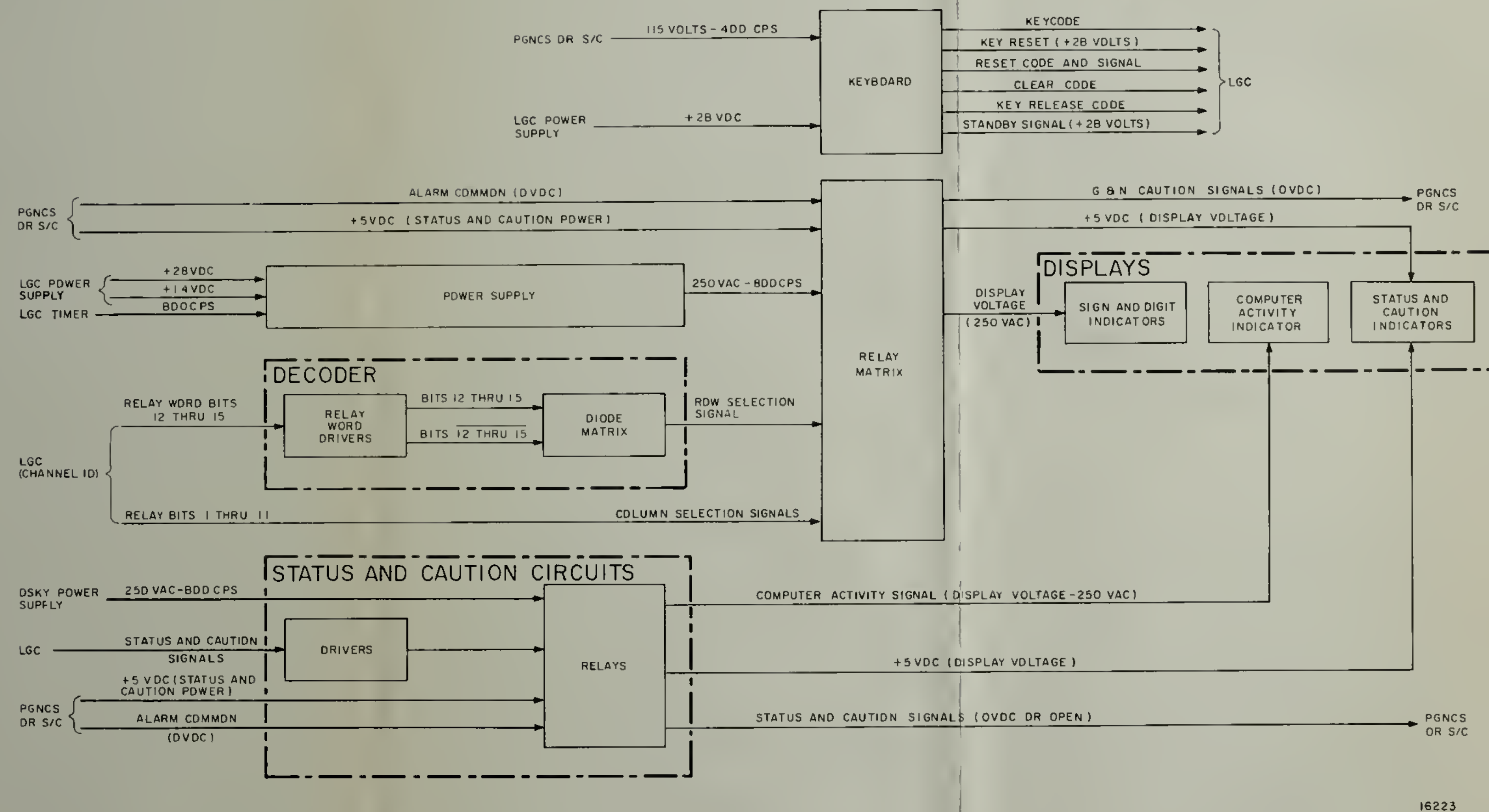

Figure 4-171. DSKY Functional Diagram

Chapter 5

MISSION OPERATIONS

5-1 SCOPE

This chapter describes the mission operations accomplished by the LEM PGNCS. These operations include lunar descent, landing, pre-launch, launch, rendezvous, and docking with the CSM. Figure 5-1 is an overall depiction of the LEM mission.

5-2 IMU COARSE ALIGNMENT

Before separation of the LEM and CSM, the gimbals in the IMU are coarse aligned using CSM position data and the LGC is synchronized with the CMC. To initiate IMU coarse alignment, the astronaut selects a precomputed alignment program in the LGC by pressing the required keys on the DSKY. (See figure 5-2). The LGC sends digital pulses, representing the required amount of change in gimbal angle, to a counter in the CDU. The CDU converts these pulses into an analog error signal applied to the gimbal servo amplifier which in turn drives the gimbal torque motors. As the gimbal angle changes, the gimbal resolver signal is applied to the CDU and converted to digital pulses. These digital pulses are used to cancel the LGC pulses stored in the CDU counter. As the counter is decremented to zero, the CDU analog error signal decreases to zero and the servo amplifier stops driving the gimbals. The CDU also sends digital pulses, representing the change in actual gimbal angles, to the LGC.

5-3 IMU FINE ALIGNMENT

After acceptable operation of all LEM systems is verified and the IMU is coarse aligned, the LEM is separated from the CSM. After separation, IMU fine alignment is initiated. (See figure 5-3.) The astronaut selects the fine alignment program in the LGC through the DSKY. The LGC commands the optical sensor to track and mark a set of stars and compares their positions with the positions of those stored in the LGC memory. The IMU gimbals, having already been coarse aligned, are at this time relatively close to their desired angles in relation to the star coordinates. To refine the gimbal angles, the LGC sends gyro torquing signals to the IMU. The CDU interprets gimbal angle analog signals, converts them to digital pulses, and relays them to the LGC as gimbal error signals. As the gimbals are being aligned, the FDAI receives total attitude information from the IMU resolvers and attitude error information from the CDU.

5-4 TRANSFER ORBIT

Prior to powered descent to the lunar surface, the LEM must descend in coasting flight to a lower altitude. A Hohmann (minimum energy) descent orbit is commanded by the LGC after the crew has requested it through the DSKY keyboard. The LGC supplies an ON discrete to the descent engine which fires until the LEM velocity has decreased by some predetermined amount. This change in velocity (ΔV) places the LEM in a new orbit with a perilune of 50,000 feet. The accelerometer loop in the IMU senses the ΔV, and when the required velocity has been reached, the LGC furnishes an OFF discrete to the descent engine.

5-5 POWERED DESCENT

5-5.1 PHASE I - BRAKING. The crew uses the DSKY to select the powered descent program in the LGC when it is apparent that the descent orbit is successful. Braking is started approximately 200 nautical miles from the point of touchdown and is terminated approximately ten nautical miles from touchdown at an altitude of approximately 11,000 feet. (See figure 5-4.) The LGC, being constantly informed by the IMU of velocity and position, sends on-off, thrust level, and gimbal trim discretes to the Descent Engine Control Assembly (DECA). The descent engine controls the rate of descent. The gimbal trim feature of the descent engine is used to control LEM trajectory and is aided by the RCS. The inertial components in the IMU sense changes in velocity and send this data to the LGC which constantly computes new thrust level commands and gimbal trim commands. The CDU converts IMU gimbal angles into digital pulses which represent LEM attitude. The FDAI presents a constant display of LEM total attitude and attitude error.

Shortly after initiation of the braking phase, the LR begins to supply forward velocity and altitude information to the LGC to supplement and update inertially derived data. The LGC displays LR data on the ALT/ALT RATE indicator on the main control panel.

5-5.2 PHASE II - FINAL APPROACH. The final approach phase is a continuation of the braking phase with the addition of supplemental manual controlling of the LEM. More credence is placed in LR data as the LEM nears the lunar surface, where this data becomes more reliable.

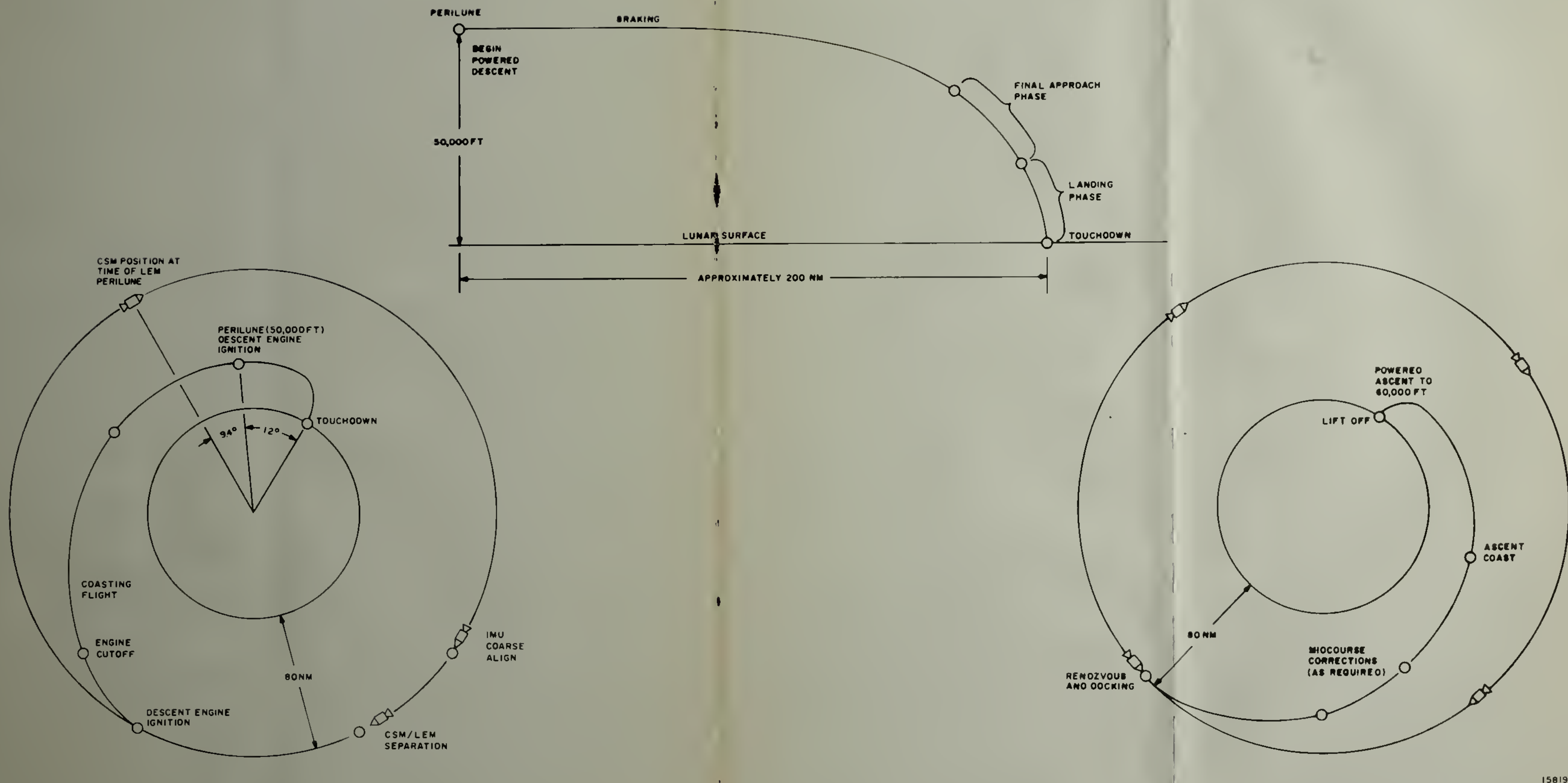

Figure 5-1. LEM Mission

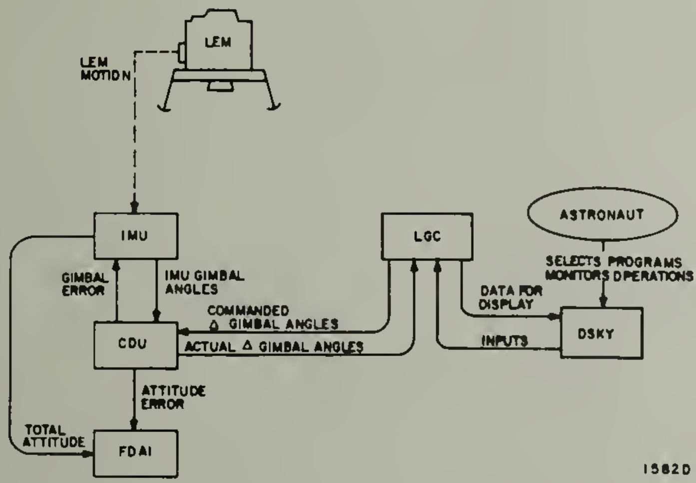

Figure 5-2. LEM IMU Coarse Alignment

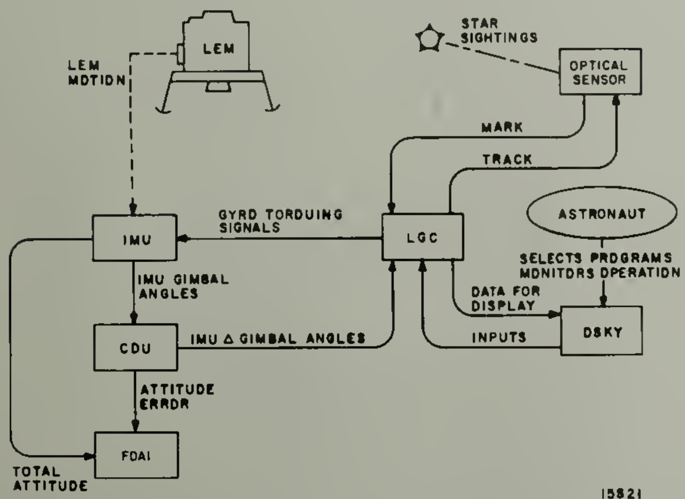

Figure 5-3. LEM IMU Fine Alignment

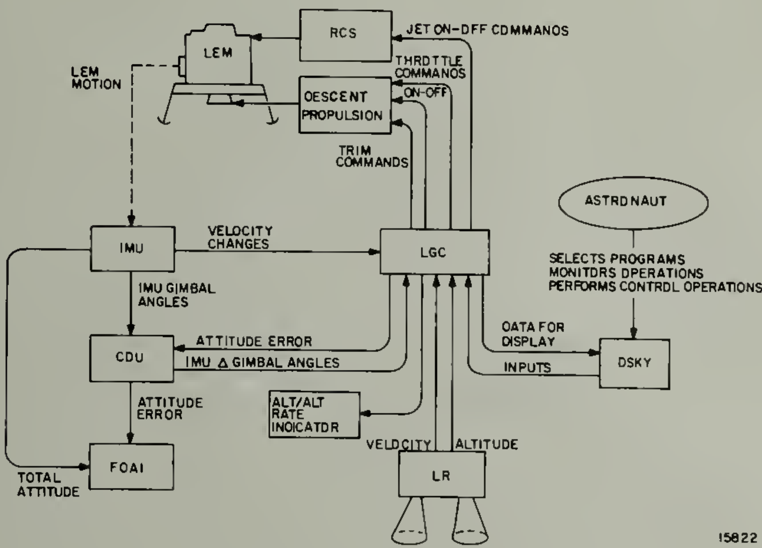

Figure 5-4. Powered Descent

Manual control of the LEM is provided by two hand controls at each crew member's station. The right hand controls, attitude controllers, are coupled through the LGC to the RCS. They are connected to the RCS in such a manner that defection of the control in any direction will fire the RCS thrusters in pairs to move the LEM about its pitch (Y), roll (Z), or yaw (X) axis. The left hand controls, integrated thrust translation controllers, serve two functions. They control translation along the LEM axes by firing the RCS thrusters and control descent by throttling the descent engine between 10 percent and 100 percent of thrust. When the two-position lever is in the JETS position, up and down movement of the control will fire a set of RCS thrusters to cause translation along the X axis. When the lever is in the THROTTLE position, up and down movement will control the thrust of the descent engine. With the lever in either position, left-right or forward-aft movement of the control will cause translation along the Y and Z axes, respectively.

NOTE: Deflection of either of the two hand controls to their limits will provide an override capability for RCS thrusting. Limit switches at all control limits are wired directly to RCS logic circuitry.

5-5.3 PHASE III - LANDING. This phase is a continuation of the final approach phase. The LEM is positioned over the desired landing spot by controlling the rate of descent, attitude, and lateral movement. The LEM positioning is accomplished automatically or, if desired, the astronaut may assume partial or complete control by utilization of the hand controls as in phase II. Engine on-off signals are issued when zero velocity and vertical attitude is achieved at an altitude of approximately three feet, allowing the LEM to free-fall to the lunar surface.

5-6 LUNAR STAY

Immediately after landing, the astronauts perform a complete checkout of all equipment required for ascent and rendezvous with the CSM. The PLSS is checked and the surrounding lunar landscape is examined before the LEM is depressurized and the hatch is opened. One astronaut exits to perform scientific experiments and gather lunar samples. Subsequent to lunar exploration, the astronauts prepare the LEM for ascent and rendezvous with the CSM. The IMU is aligned and the ascent trajectory and launch time is determined by the LGC based on the position of the orbiting CSM.

5-7 ASCENT

A powered ascent beginning with a vertical rise and followed by a pitch maneuver will be initiated at the proper time to insert the LEM into an ascent coast trajectory to intercept the orbiting CSM. The ascent engine is a constant thrust engine with a fixed nozzle; therefore, the direction of the thrust vector is determined by the attitude of the LEM which, in turn, is controlled by the RCS upon receipt of signals from the LGC. (See figure 5-5.) Throughout the powered ascent phase, the LGC receives changes in velocity from the IMU and IMU Δ angles from the CDU. The LGC calculates the attitude errors and generates signals to position the FDAI attitude error needles and to control the RCS operation. The LGC also continues to calculate the ascent engine termination time based on the relative positions of the LEM and CSM and the calculated ascent trajectory.

5-8 RENDEZVOUS AND DOCKING

During the ascent coast period, the PGNCS remains in an inertial reference condition. The LGC receives velocity changes from the IMU accelerometer loops and IMU gimbal angles from the CDU. The PGNCS continues to calculate the actual LEM coast trajectory and issue signals to the RCS to maintain the LEM on a CSM intercept trajectory. When the LEM approaches the CSM, braking thrust maneuvers are initiated by the PGNCS utilizing the RCS, to reduce the velocity between the LEM and CSM to zero. The astronaut will then utilize the hand controls to perform the required docking maneuvers. The required thrusting during these maneuvers will be provided by the RCS.

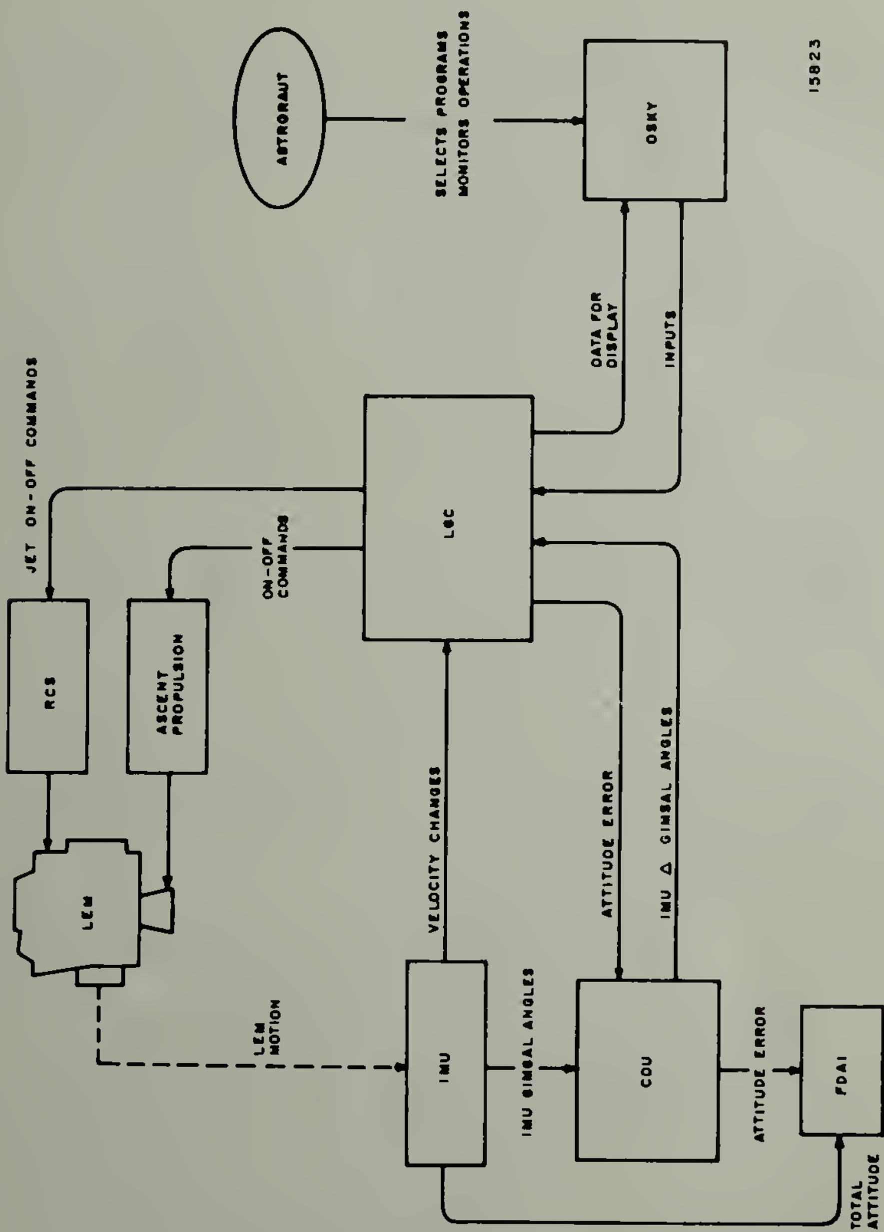

Figure 5-5. Powered Ascent

Chapter 6

CHECKOUT AND MAINTENANCE EQUIPMENT

6-1 SCOPE

This chapter contains a list of test equipment and tools necessary to complete checkout of the LEM PGNCS and the PGNCS subsystems. The test equipment is listed in alphabetical order in table 6-I. The tools are listed in alphabetical order in table 6-II. Operation and front panel calibration procedures for the GSE are contained in the job description cards (JDC's) listed in table 6-III. The layout of equipment in a typical universal test station is shown in figure 6-1. The test station is environmentally controlled and provides for precision checkout of the PGNCS and the PGNCS subsystems.

Table 6-I. Checkout and Maintenance Test Equipment

Equipment and Part Number	Short Nomenclature	Description and Use
Apollo guidance computer (AGC) auxiliary calibration console, 2014059-011	Auxiliary calibration system	Checks calibration of LGC clock oscillator.
AGC CTS operation console, 2014024-011	AGC/OC	Provides mounting and cooling surfaces, power and test connections for checking out CSS.
AGC/GSE interconnect set, PGNCS, 2014255-011	AGC/GSE interconnect cables, PGNCS	Provides cables and buffer circuits to interconnect LGC to GSE during PGNCS checkout.

(Sheet 1 of 5)

Table 6-I. Checkout and Maintenance Test Equipment

Equipment and Part Number	Short Nomenclature	Description and Use
AGC/GSE interconnect set, subsystem, 2014268-011	AGC/GSE interconnect cables, CSS	Provides cables and mounting bracket to interconnect LGC to GSE during CSS checkout.
AGC handling fixture, 2014282-011	AGC handling fixture	Provides mounting and protection for LGC prior to installation and during handling.
AGC test set, 2014042-011	Computer test set (CTS)	Checks operation of CSS.
AGC universal DSKY handling fixture 2014013-011	DSKY handling fixture	Provides protection and handling capability of DSKY during transfer, test, and storage. Also provides a means of mounting the DSKY in the AGC/OC.
AGC calibration system console, 2014099-011	Calibration system	Checks calibration of LGC clock oscillator and provides frequency reference to auxiliary calibration system.
Component mounting plate, 6900007-011	Component mounting plate	Provides support and cooling capability for LGC, CDU, and PSA during testing.
Computer simulator, 2014048-011	Computer simulator	Simulates LGC signals, loads, and outputs for ISS checkout.
Connector cover set, 6900001-011	Connector covers	Provides protection for electrical connectors of PGNCS harness.
Degausser, 1900299-021	Degausser	Demagnetizes ducosyns of 16 PIP's and 25 IRIG's during ISS checkout.
Display and keyboard pedestal mount, 2014014-011	DSKY pedestal mount	Provides housing and mounting for DSKY during PGNCS test.

(Sheet 2 of 5)

Table 6-I. Checkout and Maintenance Test Equipment

Equipment and Part Number	Short Nomenclature	Description and Use
G and N transport cart, 1900009-031	G and N transport cart	Used for local transportation of PGNCS components.
G and N coolant and power console, 1902134-021	Coolant and power console	Provides cooling, power and precision voltage monitoring during PGNCS and ISS checkout.
GSE coolant interconnect hose set, ISS/OSS, 2900405-011	GSE coolant hoses	Connects PGNCS components and coldplates to coolant and power console.
GSE distribution box, 2900024-011	GSE distribution box	Provides test interconnection for use during PGNCS and subsystem checkout.
IMU lifting fixture, 2900064-011	IMU lifting fixture	Provides means of positioning IMU and IMU mounting fixture on rotary table.
IMU lifting temperature controller, 2900063-011	IMU lifting temperature controller	Provides heater power to IMU inertial components during LEM stacking.
IMU mounting fixture, 2900000-011	IMU mounting fixture	Mounts IMU to rotary table for ISS checkout.
IMU pressure seal tester 1900804-011	IMU pressure seal tester	Checks for leakage of pressure seals in IMU case during PGNCS checkout.
IMU snap-on bellows, 1900802-011	IMU snap-on bellows	Allows for expansion of coolant in IMU case during transportation when filled.
Interconnect cable set, 2900025-011	Interconnect cables	Interconnects PGNCS components and GSE during PGNCS and subsystem checkout.
Interconnect cable set, 6900043-011	Interconnect cables	Interconnects PGNCS components and GSE during PGNCS and subsystem checkout.

(Sheet 3 of 5)

Table 6-I. Checkout and Maintenance Test Equipment

Equipment and Part Number	Short Nomenclature	Description and Use
Lifting battery pack, 2900812-011	Lifting battery pack	Part of IMU lifting temperature controller to provide backup heater power.
Optics cleaning kit, 1019984-011	Optics cleaning kit	Used to clean LORS optics.
Optics-inertial analyzer, 2900023-011	OIA	Provides control signals and monitoring and measurement facilities for PGNCS and subsystem checkout.
Oscillograph console, 1900000-021	Oscillograph	Monitors and records signals from OIA.
Portable temperature controller, 2900060-011	PTC	Provides power for IMU temperature control when normal power is not applied.
PSA adapter module	PSAAM	Buffer between PGNCS and ACE for post-installation testing.
PSA test point adapter, 2900037-011	PSA test point adapter	Provides test interconnections for use with OIA for monitoring purposes.
Programmer and monitor interconnect set, 2014064-011	P and M interconnect set	Provides extra set of cables to connect CTS to buffer circuit assembly at a universal test station.
PTA/PEA mounting fixture, 2900066-011	PTA/PEA mounting fixture	Provides mounting for PTA on rotary table during PGNCS and ISS testing.
PTA/PEA test point adapter, 2900145-011	PTA/PEA test point adapter	Provides signal select capability for monitoring signals from PTA during PGNCS and ISS testing.
Purging and filling fixture, 1902371-011	Purging and filling fixture	Purges and fills IMU and GSE coldplates requiring coolant.

(Sheet 4 of 5)

Table 6-I. Checkout and Maintenance Test Equipment

Equipment and Part Number	Short Nomenclature	Description and Use
Resolver circuit tester, 2900708-011	Resolver Circuit tester	Provides simulated resolver signals and monitoring facilities for testing PGNCS resolver circuits.
Rotary table, 1900926-021	Rotary table	Serves as a mounting and test platform for selected PGNCS components during PGNCS and ISS testing.
Rotary table calibration set, 1900810-011	Rotary table calibration set	Contains all equipment necessary to perform rotary table calibration.
Subsystem mounting fixture, 2900070-011	Subsystem mounting fixture	Supports portions of PGNCS and GSE during ISS and PGNCS testing.

(Sheet 5 of 5)

Table 6-II. Checkout and Maintenance Tools

Equipment and Part Number	Short Nomenclature	Description and Use
AGC sling; MY-4 Abbot Jordan Hoist Co., Brighton, Mass.	computer sling	Connects lifting hoists to LGC when transporting LGC outside of LGC shipping container.
Allen adapter; 5/32 inch, JO Line, or equivalent	allen adapter	Adapts torque wrench to LGC module inserts.

(Sheet 1 of 2)

Table 6-II. Checkout and Maintenance Tools

Equipment and Part Number	Short Nomenclature	Description and Use
Torque wrench; 17 inch-pound, JO Line, or equivalent	torque wrench	Torque LGC modules onto LGC trays.
IMU sling; 1015458	IMU sling	Connects lifting hoist to IMU to position and remove IMU from rotary table during ISS or PGNCS checkout.
Tool kit	tool kit	Contains general usage tools required to support maintenance activities in G and N laboratory and stockroom.

(Sheet 2 of 2)

Table 6-III. List of Operating Procedure JDC's for GSE

Equipment	JDC Number	JDC Description
Coaxial distribution panel	18004	Operating primary signal selector panel, coaxial distribution panel, and PSA test point adapter to apply auxiliary signals to dual beam oscilloscope.
Counter	18017	Operating counter as a forward or reverse counter.
Counter	18018	Operating counter to count number of input events that occur during any preselected time interval.
Counter	18019	Operating counter to count number of input events during interval determined by "D" input events.

(Sheet 1 of 5)

Table 6-III. List of Operating Procedure JDC's for GSE

Equipment	JDC Number	JDC Description
Counter	18020	Operating counter to count clock frequency pulses during interval determined by "D" input events.
Counter	18021	Test to determine correct operation of N_1 switches, time base circuitry, and count-chain circuitry (counter operation).
Counter	18022	Test to determine correct operation of N_2 switch (counter operation).
Counter-timer	05401	Operating counter to measure frequency.
Counter-timer (CTS)	05402	Operating counter-timer to count pulses during a time interval.
Counter-timer (CTS)	05403	Operating counter-timer to measure period between leading edges of pulses.
Counter-timer (CTS)	05404	Operating counter-timer to measure time between pulses using internal frequency standard.
Digital recorder	18043	Operating and interpreting digital recorder.
Digital voltmeter	18035	Operating digital voltmeter to measure a dc voltage.
Digital voltmeter	18036	Operating digital voltmeter to measure an ac voltage.
Digital voltmeter	18037	Operating digital voltmeter to automatically measure an ac or dc voltage.
Dual beam oscilloscope	18005	Operating dual beam oscilloscope, scope "A", upper beam differential amplifier, and primary signal selector panel to measure voltages.

(Sheet 2 of 5)

Table 6-III. List of Operating Procedure JDC's for GSE

Equipment	JDC Number	JDC Description
Dual beam oscilloscope	18006	Operating dual beam oscilloscope upper beam differential amplifier to measure phase shift.
Dual beam oscilloscope	18007	Operating dual beam oscilloscope to make time measurements.
Dual beam oscilloscope	18008	Operating dual beam oscilloscope to make frequency measurements.
Dual beam oscilloscope	18009	Operating dual beam oscilloscope, scope "B", channel 1 to monitor pulses.
Dual beam oscilloscope	18010	Instructions for applying two signals simultaneously to dual beam oscilloscope, scope "B".
Dual beam oscilloscope	18011	Instructions for applying an oscillograph signal to dual beam oscilloscope, scope "B", channel 12.
Electronic counter (calibration system)	05400	Operating counter to measure frequency.
Galvanometer and current source monitor	18016	Operating galvanometer and current source monitor panel to measure voltages.
G and N coolant and power console	18046	Operating and interconnecting G and N coolant and power console for PGNCS testing.
Gimbal position control panel	18044	Operating gimbal position control panel.
Oscillograph console	18023	Operating oscillograph (electric writing)
Oscillograph console	18024	Operating oscillograph (ink writing)

(Sheet 3 of 5)

Table 6-III. List of Operating Procedure JDC's for GSE

Equipment	JDC Number	JDC Description
Oscillograph console	18025	Adjustment of oscillograph console dc amplifiers.
Oscillograph console	18026	Operating oscillograph console dc amplifiers.
Oscillograph console	18027	Adjustment of oscillograph console phase sensitive demodulators (800 cps, reference) (normal operation).
Oscillograph console	18028	Adjustment of oscillograph console phase sensitive demodulators (3200 cps reference) (normal operation).
Oscillograph console	18029	Adjustment of oscillograph console phase sensitive demodulators (800 cps reference) (periodic phase shift check and operation).
Oscillograph console	18031	Operating oscillograph console phase sensitive demodulators.
Oscillograph console	18032	Installation of new ink cartridge in oscillograph console.
Oscillograph console	18033	Installation of new ink pen in oscillograph console.
Oscillograph console	18034	Installation of new paper in oscillograph console.
Oscilloscope (CTS)	05405	Operating oscilloscope to measure pulse characteristics.
Phase angle voltmeter	18038	Operating phase angle voltmeter to measure total rms voltage.
Phase angle voltmeter	18039	Operating phase angle voltmeter to measure fundamental rms voltage.

(Sheet 4 of 5)

Table 6-III. List of Operating Procedure JDC's for GSE

Equipment	JDC Number	JDC Description
Phase angle voltmeter	18040	Operating phase angle voltmeter to measure a phase angle.
Phase angle voltmeter	18041	Operating phase angle voltmeter to measure in-phase and quadrature components.
Phase angle voltmeter	18042	Operating phase angle voltmeter to indicate a phase sensitive null.
Primary signal selector panel	18000	Operating primary signal selector panel to apply internal signals to digital voltmeter, phase angle voltmeter and dual beam oscilloscope.
Primary signal selector panel	18001	Operating primary signal selector panel to apply reference signals to dual beam oscilloscope.
Primary signal selector panel	18002	Operating primary signal selector panel to apply PSA test point adapter test point signals to digital voltmeter, phase angle voltmeter, and dual beam oscilloscope.
Primary signal selector panel	18003	Operating primary signal selector panel to apply auxiliary signals to digital voltmeter, phase angle voltmeter, and dual beam oscilloscope.
Filling and purging fixture	18045	Operating filling and purging fixture to purge and fill PGNCS components and GSE coldplates.
Signal generator	18012	Adjustment of signal generator.
Signal generator	18013	Operating signal generator.

(Sheet 5 of 5)

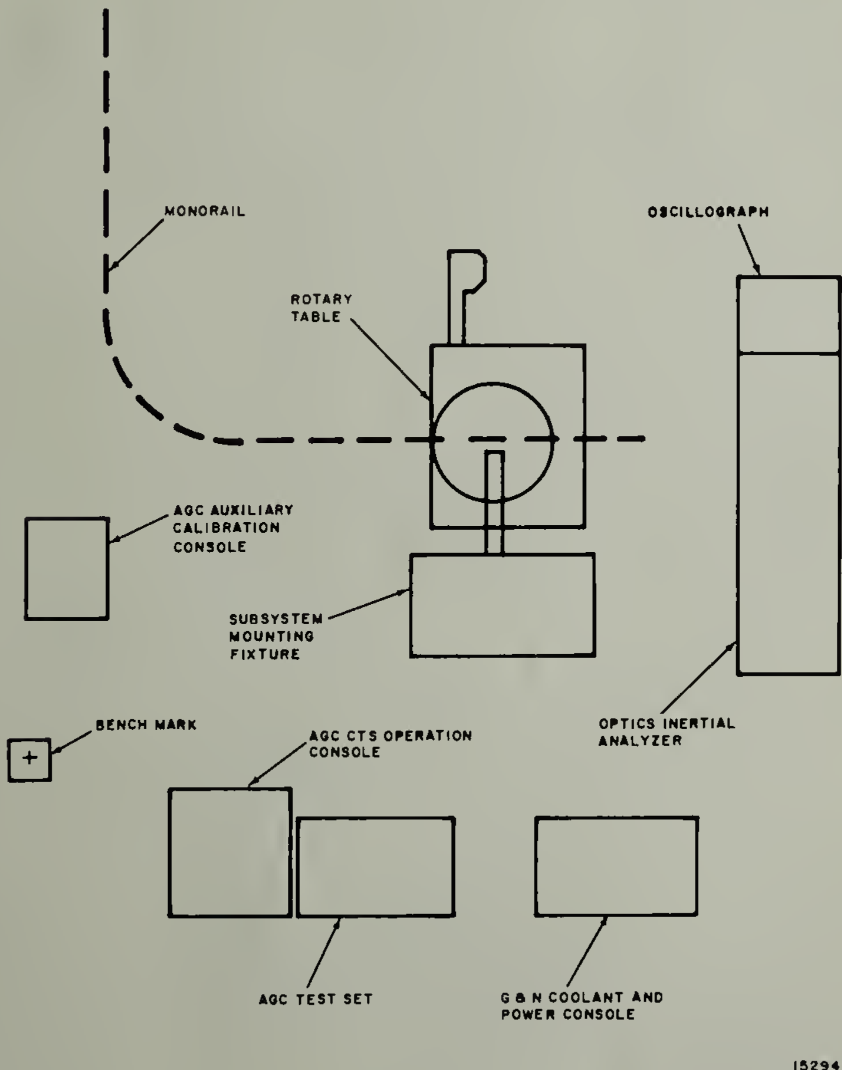

Figure 6-1. Typical Universal Test Station Layout

Chapter 7

CHECKOUT

7-1 SCOPE

This chapter contains flowgrams which outline checkout procedures for the LEM PGNCS and the PGNCS subsystems. Checkout is performed at the G and N laboratories of North American Aviation (NAA), Kennedy Space Center (KSC), Grumman Aircraft Engineering Coproration (GAEC), and the Manned Spacecraft Center (MSC). A master flowgram for the PGNCS and one for each of the PGNCS subsystems precedes more detailed preparation and checkout flowgrams. Each master flowgram references the detailed flowgrams which, in turn, reference the job description cards (JDC's) required to fulfill the checkout function. The detailed flowgrams also refer to JDC's which describe setup and operation of GSE.

Information regarding packing, shipping and handling of any component of the PGNCS will be found in Packing, Shipping, and Handling Manual, ND-1021038.

7-2 PRIMARY GUIDANCE, NAVIGATION AND CONTROL SYSTEM

7-2.1 PREPARATION. Table 7-I lists PGNCS components and GSE required for PGNCS and subsystem checkout. Table 7-II lists required system and GSE interconnect cabling.

7-2.2 CHECKOUT. The PGNCS master flowgram (figure 7-1) specifies the conditions leading to a PGNCS checkout and displays the mandatory sequence to be followed. Detailed flowgrams (figures 7-2 and 7-3) give sequential listings of JDC's to be performed.

7-2.3 TEST DESCRIPTIONS. This paragraph will provide detailed descriptions of the PGNCS checkout tests as performed by using the JDC's and will be supplied upon final definition of the checkout requirements and procedures.

7-3 INERTIAL SUBSYSTEM

7-3.1 PREPARATION. Table 7-III lists the cables and interconnections required of the ISS. Refer to Table 7-I for a listing of PGNCS components and GSE necessary to perform an ISS test.

7-3.2 CHECKOUT. The ISS master flowgram (figure 7-4) specifies the conditions leading to an ISS checkout. Detailed flowgrams (figures 7-5 and 7-6) give sequential listings of JDC's to be performed.

7-4 COMPUTER SUBSYSTEM

7-4.1 PREPARATION. Refer to Table 7-I for a listing of PGNCS components and GSE required to perform a CSS checkout. Table 7-IV lists the cables and interconnections used to connect the CSS and GSE during CSS checkout.

7-4.2 CHECKOUT

(To be supplied.)

7-5 LEM OPTICAL RENDEZVOUS SUBSYSTEM

(To be supplied.)

Table 7-I. Equipment Required for Checkout

Equipment	Part Number	Used in		
		PGNCS	ISS	CSS
PGNCS COMPONENTS				
CDU	2007222-041	X	X	
PGNCS interconnect harness	6014515-011	X		
IMU and PTA	6007001-011	X	X	
LGC	2003100-021	X		X
DSKY	2003985-031	X		X
PSA	6007200-011	X	X	
Signal conditioner module		X		
GSE				
AGC/GSE interconnect cables, PGNCS	2014255-011	X		
AGC/GSE interconnect cables, CSS	2014268-011			X

(Sheet 1 of 3)

Table 7-I. Equipment Required for Checkout

Equipment	Part Number	Used in PGNCS	Used in ISS	Used in CSS
AGC handling fixture	2014282-011	X		X
AGC/OC	2014024-011			X
Auxiliary calibration system	2014059-011			X
Calibration system	2014099-011			X
Component mounting plate	6900007-011	X	X	
Computer simulator	2014048-011		X	
Coolant and power console	1902134-021	X	X	
Connector covers	6900001-011	X	X	
CTS	2014042-011	X		X
Degausser	1900299-021	X	X	
DSKY handling fixture	2014013-011	X		X
DSKY pedestal mount	2014014-011	X		
G and N transport cart	1900009-031	X	X	
GSE coolant hoses	2900405-011	X	X	
GSE distribution box	2900024-011	X	X	
IMU lifting fixture	2900064-011	X	X	
IMU lifting temperature controller	2900063-011	X	X	
IMU mounting fixture	2900000-011	X	X	
IMU pressure seal tester	1900804-011	X		
IMU snap-on bellows	1900802-011	X	X	
Interconnect cables	2900025-011	X	X	
Interconnect cables	6900043-011	X	X	
OIA	2900023-011	X	X	
Oscillograph	1900000-021	X	X	
P and M interconnect set	2014064-011	X		X

(Sheet 2 of 3)

Table 7-I. Equipment Required for Checkout

Equipment	Part Number	Used in		
		PGNCS	ISS	CSS
PSA test point adapter	2900037-011	X	X	
PTA/PEA mounting fixture	2900066-011	X	X	
PTA/PEA test point adapter	2900145-011	X	X	
Purging and filling fixture	1902371-011	X	X	
Rotary table	1900926-021	X	X	
Rotary table calibration set	1900810-011	X	X	
Subsystem mounting fixture	2900070-011	X	X	

(Sheet 3 of 3)

Table 7-II. PGNCS Interconnect Cables

Cable	Part Number	Terminations (Plug/Jack)	Equipment
W1	1900886	P1/J1 P2/J1	OIA Oscillograph
W2	1900669	P1/J2 P2/J2	OIA Oscillograph
W3	1900670	P1/J3 P2/J3	OIA Oscillograph
W4	1900671	P1/J4 P2/J4	OIA Oscillograph
W19	1900873	P1/J20 P2/J3	OIA Coolant and power console
W22	1900959	P1/J23 P2/J5	OIA CTS

(Sheet 1 of 6)

Table 7-II. PGNCS Interconnect Cables

Cable	Part Number	Terminations (Plug/Jack)	Equipment
W26	1900921	P1/A30J1 P2/facility	OIA Wall power
W27	1900871	P1/A30J2 P2/J1	OIA Coolant and power console
W28	1900872	P1/J2 P2/facility	Coolant and power console Wall power
W33	1901404	P1/E1 P2/E4	OIA Oscillograph
W37	1901662	P1/facility P2/E300	Facility ground Rotary table
W64	1901676	P1/E1 P2/E300	G and N mounting fixture base Rotary table
W65	1900739	P1/J4 P2/J15	Current source monitor PTA test point adapter
W85	1901960	P1/A30J5 P2/facility	OIA Emergency wall power
W120	2900456	P1/J19 P2/56J1	OIA PGNCS interconnect harness B
W121	2900257	P1/J8 P2/J9 P3/J13 P4/J14 P5/J15 P6/J57	OIA OIA OIA OIA OIA GSE distribution box
W122	2900378	P1/J18 P2/J17 P3/J16 P4/J22 P5/J55 P6/J59 P7/J62 P8/J58	OIA OIA OIA OIA GSE distribution box GSE distribution box GSE distribution box GSE distribution box

(Sheet 2 of 6)

Table 7-II. PGNCS Interconnect Cables

Cable	Part Number	Terminations (Plug/Jack)	Equipment
W123	2900379	P1/J21	OIA
		P2/J24	OIA
		P3/J25	OIA
		P4/J26	OIA
		P5/J60	GSE distribution box
		P6/J63	GSE distribution box
		P7/J66	GSE distribution box
		P8/J67	GSE distribution box
W124	2900380	P1/J5	OIA
		P2/J6	OIA
		P3/J7	OIA
		P4/J64	GSE distribution box
		P5/J61	GSE distribution box
		P6/J65	GSE distribution box
W125	2900186	P1/J28	OIA
		P2/J29	OIA
		P3/J30	OIA
		P4/J50	GSE distribution box
		P5/J51	GSE distribution box
		P6/J54	GSE distribution box
W126	2900381	P1/J10	OIA
		P2/J11	OIA
		P3/J12	OIA
		P4/J52	GSE distribution box
		P5/J53	GSE distribution box
		P6/J56	GSE distribution box
W127 (2 required)	2900327	First cable connected between E1 on OIA and E300 on rotary table. Second cable connected between E80 on OIA and E1 on GSE distribution box.	
W128 (2 required)	2900458	First cable connected between E2 on GSE distribution box and E300 on rotary table. Second cable connected between E1 on subsystem mounting fixture and E300 on rotary table.	

(Sheet 3 of 6)

Table 7-II. PGNCS Interconnect Cables

Cable	Part Number	Terminations (Plug/Jack)	Equipment
W129 (2 required)	2900459	First cable connected between E1 on subsystem mounting fixture and E3 on GSE distribution box.	
		Second cable connected between E1 on subsystem mounting fixture and E2 on subsystem mounting fixture.	
W130	2900460	Connected between E1 on coolant and power console and E300 on rotary table.	
W131	6900023	P1/J13	GSE distribution box
		P2/J16	GSE distribution box
		P3/56P12	PGNCS interconnect harness A
		P4/56P10	PGNCS interconnect harness A
		P5/56P6	PGNCS interconnect harness A
		P6/56P7	PGNCS interconnect harness A
		P7/J2	CTS
		P8/J3	CTS
		/E1	Subsystem mounting fixture
W132	2900497	P1	Not used
		P2/56P16	PGNCS interconnect harness A
		P3/56P17	PGNCS interconnect harness A
		P4/56P15	PGNCS interconnect harness A
		P5/J2	PTA test point adapter
		P6	Not used
		P7/56P14	PGNCS interconnect harness B
		P8/56P11	PGNCS interconnect harness B
		P9/J14	GSE distribution box
		P10/J18	GSE distribution box
W134	2900588	P1/56P18	PGNCS interconnect harness B
		P2/56P13	PGNCS interconnect harness A
W135	6900024	P1/J27	GSE distribution box
		P2/P1	Reticle dimming assembly
		P3/J1	Reticle dimming assembly
W136	2900461	P1/J24	GSE distribution box
		P2/J28	GSE distribution box
		P3/J3	PSA test point adapter
		P4/J4	PSA test point adapter

(Sheet 4 of 6)

Table 7-II. PGNCS Interconnect Cables

Cable	Part Number	Terminations (Plug/Jack)	Equipment
W137	6900005	P1/J33 J1/56P8	GSE distribution box PGNCS interconnect harness A
W138	6900040	P1/J26 P2/A	GSE distribution box Sig cond module brk-out box
W139	6900004	P1/J15 P2/56P9	GSE distribution box PGNCS interconnect harness A
W140	2900457	P1/J4 P2/J34	Coolant and power console GSE distribution box
W141	2900591	P1/A1J3 P2/J1 P3/J2 P4/J1 P5/J1 P6/J1	GSE distribution box IMU PTA coldplate LGC coldplate CDU coldplate PSA coldplate
W142	6900041	P1/B or P1/P2 P2/J1 P3/J2	Sig cond module brk-out box or W157 PSA test point adapter PSA test point adapter
W143	6900025	P1/ P2/J29 P3/56P5	DSKY OIA PGNCS interconnect harness A
W144	6900006	P1/J1 P2/35A2J18	PTA test point adapter PTA
W157	6900045	P1/ P2/P1	Signal conditioner module W142
W226	2014137-011	P1/Test Conn. P2/J4 P3/J5 P4/J6	LGC Buffer circuit assembly Buffer circuit assembly Buffer circuit assembly
W232	2014484-011	P1/J2 J4/P6 P2/J2 P3/J7	G and N mounting fixture W259 CTS CTS

(Sheet 5 of 6)

Table 7-II. PGNCS Interconnect Cables

Cable	Part Number	Terminations (Plug/Jack)	Equipment
W233	2014483-011	P1/J2 P2/J16 P3/J10 P4/J4	G and N mounting fixture CTS CTS CTS
W236	2014463-011	P1/J1 P2/J5	Buffer circuit assembly CTS
W237	2014462-011	P1/J2 P2/J11	Buffer circuit assembly CTS
W238	2014462-021	P1/J3 P2/J17	Buffer circuit assembly CTS
W239	2014462-031	P1/J9 P2/J18	Buffer circuit assembly CTS
W259	2014470-011	P1/CP1 P2/ P3/ P4/J7 P5/J8 P6/J4 P7 P8	Calibration system Digital ohmmeter Digital ohmmeter Buffer circuit assembly Buffer circuit assembly W232 Digital ohmmeter Digital ohmmeter

(Sheet 6 of 6)

Table 7-III. Inertial Subsystem Interconnect Cables

Cable	Part Number	Terminations (Plug/Jack)	Equipment
W1	1900886	P1/J1 P2/J1	OIA Oscillograph
W2	1900669	P1/J2 P2/J2	OIA Oscillograph

(Sheet 1 of 5)

Table 7-III. Inertial Subsystem Interconnect Cables

Cable	Part Number	Terminations (Plug/Jack)	Equipment
W3	1900670	P1/J3 P2/J3	OIA Oscillograph
W4	1900671	P1/J4 P2/J4	OIA Oscillograph
W19	1900873	P1/J20 P2/J3	OIA Coolant and power console
W26	1900921	P1/A30J1 P2/facility	OIA Wall power
W27	1900871	P1/A30J2 P2/J1	OIA Coolant and power console
W28	1900872	P1/J2 P2/facility	Coolant and power console Wall power
W33	1901404	P1/E1 P2/E4	OIA Oscillograph
W37	1901662	P1/facility P2/E300	Facility ground Rotary table
W64*	1901676	P1/E1 P2/E300	G and N mounting fixture Rotary table
W65	1900739	P1/J4 P2/J15	Current source monitor PTA test point adapter
W85	1901960	P1/A30J5 P2/facility	OIA Emergency wall power
W120	2900456	P1/J19 P2/J1	OIA W146
W121	2900257	P1/J8 P2/J9 P3/J13 P4/J14 P5/J15 P6/J57	OIA OIA OIA OIA OIA GSE distribution box

* Not used at GAEC

(Sheet 2 of 5)

Table 7-III. Inertial Subsystem Interconnect Cables

Cable	Part Number	Terminations (Plug/Jack)	Equipment
W122	2900378	P1/J18	OIA
		P2/J17	OIA
		P3/J16	OIA
		P4/J22	OIA
		P5/J55	GSE distribution box
		P6/J59	GSE distribution box
		P7/J62	GSE distribution box
		P8/J58	GSE distribution box
W123	2900379	P1/J21	OIA
		P2/J24	OIA
		P3/J25	OIA
		P4/J26	OIA
		P5/J60	GSE distribution box
		P6/J63	GSE distribution box
		P7/J66	GSE distribution box
		P8/J67	GSE distribution box
W124	2900380	P1/J5	OIA
		P2/J6	OIA
		P3/J7	OIA
		P4/J64	GSE distribution box
		P5/J61	GSE distribution box
		P6/J65	GSE distribution box
W125	2900186	P1/J28	OIA
		P2/J29	OIA
		P3/J30	OIA
		P4/J50	GSE distribution box
		P5/J51	GSE distribution box
		P6/J54	GSE distribution box
W126	2900381	P1/J10	OIA
		P2/J11	OIA
		P3/J12	OIA
		P4/J52	GSE distribution box
		P5/J53	GSE distribution box
		P6/J56	GSE distribution box

(Sheet 3 of 5)

Table 7-III. Inertial Subsystem Interconnect Cables

Cable	Part Number	Terminations (Plug/Jack)	Equipment
W127 (2 required)	2900327	First cable connected between E1 on OIA and E300 on rotary table.	
		Second cable connected between E80 on OIA and E1 on GSE distribution box.	
W128 (2 required)	2900458	First cable connected between E2 on GSE distribution box and E300 on rotary table.	
		Second cable connected between E1 on subsystem mounting fixture and E300 on rotary table.	
W129 (2 required)	2900459	First cable connected between E1 on subsystem mounting fixture and E3 on GSE distribution box.	
		Second cable connected between E1 on subsystem mounting fixture and E2 on subsystem mounting fixture.	
W130	2900460	P1/E1	Coolant and power console
		P2/E300 .	Rotary table
W132	2900497	P1	Not used
		P2/P16	W146
		P3/P17	W146
		P4/P15	W146
		P5/J2	PTA test point adapter
		P6	Not used
		P7/J10	GSE distribution box
		P8/J17	GSE distribution box
		P9/J14	GSE distribution box
		P10/J18	GSE distribution box
W133	6900044	P1/J11	GSE distribution box
		P2/	PSA
		P3/	CDU
		P4/J12	GSE distribution box
		P5/J16	GSE distribution box
		P6/J15	GSE distribution box
		P7/J23	GSE distribution box
		P8/J19	GSE distribution box

(Sheet 4 of 5)

Table 7-III. Inertial Subsystem Interconnect Cables

Cable	Part Number	Terminations (Plug/Jack)	Equipment
W133 (cont)		P9/J20	GSE distribution box
		P10/J33	GSE distribution box
		P11/J26	GSE distribution box
		P12/J1	PSA test point adapter
		P13/J215	Subsystem mounting fixture
		P14/J2	PSA test point adapter
W134	2900588	P1/P18	W146
		P2/J215	Subsystem mounting fixture
W136	2900461	P1/J24	GSE distribution box
		P2/J28	GSE distribution box
		P3/J3	PSA test point adapter
		P4/J4	PSA test point adapter
W140	2900457	P1/J4	Coolant and power console
		P2/J34	GSE distribution box
W141	2900591	P1/A1J3	GSE distribution box
		P2/J1	IMU
		P3/J2	PTA coldplate
		P4/J1	Not used
		P5/J1	CDU coldplate
		P6/J1	PSA coldplate
W144	6900006	P1/J1	PTA test point adapter
		P2/35A2J18	PTA
W146	2900351	P15/P4	W132
		P16/P2	W132
		P17/P3	W132
		P18/P1	W134
		P19/35A2J19	PTA
		P20/J2	IMU
		P21/J1	IMU
		J1/P2	W120

(Sheet 5 of 5)

Table 7-IV. Computer Subsystem Interconnect Cables

Cable	Part Number	Terminations (Plug/Jack)	Equipment
W212	1006482-011	P1/J7 P2/J1	AGC/OC CTS
W213	1006482-002	P1/J8 P2/J7	AGC/OC CTS
W214	1006482-003	P1/J9 P2/J13	AGC/OC CTS
W215	1006482-004	P1/J4 P2/J2	AGC/OC CTS
W216	1006482-005	P1/J5 P2/J8	AGC/OC CTS
W217	1006482-006	P1/J6 P2/J14	AGC/OC CTS
W218	1006482-007	P1/J11 P2/J3	AGC/OC CTS
W219	1006482-008	P1/J12 P2/J9	AGC/OC CTS
W220	1006482-009	P1/J10 P2/J15	AGC/OC CTS
W221	1006482-010	P1/J1 P2/J10	AGC/OC CTS
W222	1006482-011	P1/J2 P2/J16	AGC/OC CTS
W223	1006482-012	P1/J3 P2/J4	AGC/OC CTS
W225	2014486-011	P1/J9 P2/J3	DSKY AGC/OC
*W226	2014137-011	P1/Test Conn. P2/J4 P3/J5 P4/J6	LGC Buffer circuit assembly Buffer circuit assembly Buffer circuit assembly

*This cable part of G and N Test Interconnection Set (2014255-011)

(Sheet 1 of 2)

Table 7-IV. Computer Subsystem Interconnect Cables

Cable	Part Number	Terminations (Plug/Jack)	Equipment
W227	2014199-011	P1/S/C Conn.	LGC
		P2/J2	AGC/OC junction panel assembly
		P3/J3	AGC/OC junction panel assembly
		P4/J4	AGC/OC junction panel assembly
		P5/J5	AGC/OC junction panel assembly
		P6/J1	AGC/OC junction panel assembly
*W236	2014463-011	P1/J1	Buffer circuit assembly
		P2/J5	CTS
*W237	2014462-011	P1/J2	Buffer circuit assembly
		P2/J1	CTS
*W238	2014462-021	P1/J3	Buffer circuit assembly
		P2/J17	CTS
*W239	2014462-031	P1/J9	Buffer circuit assembly
		P2/J18	CTS
*W259	2014470-011	P1/CP1	Calibration system
		P2	Digital ohmmeter
		P3	Digital ohmmeter
		P4/J7	Buffer circuit assembly
		P5/J8	Buffer circuit assembly
		P6/J6	AGC/OC junction panel assembly
		P7	Digital ohmmeter
		P8	Digital ohmmeter

*These cables part of G and N Test Interconnection Set (2014255-011)

(Sheet 2 of 2)

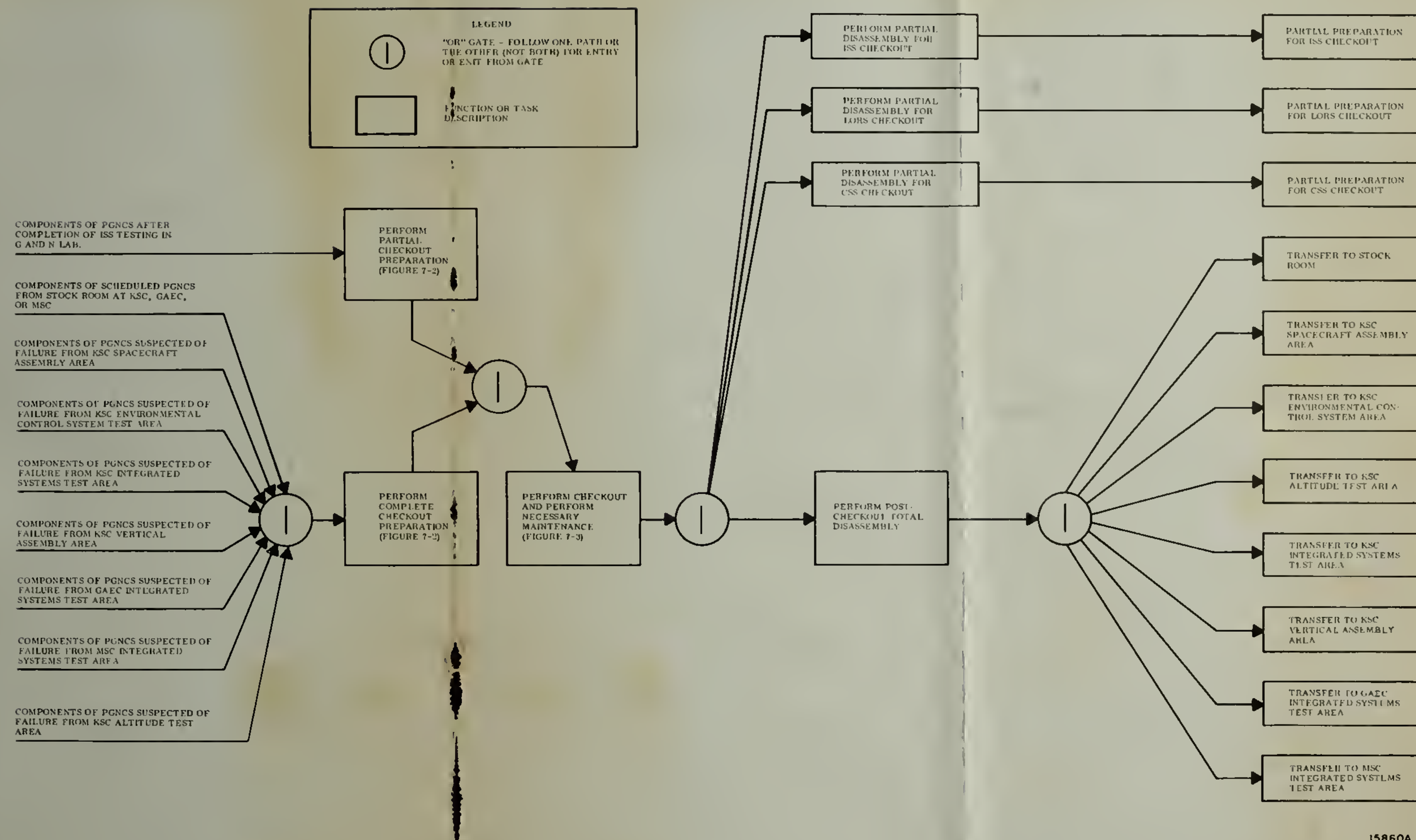

Figure 7-1. Primary Guidance, Navigation, and Control System Master Checkout Flowgram

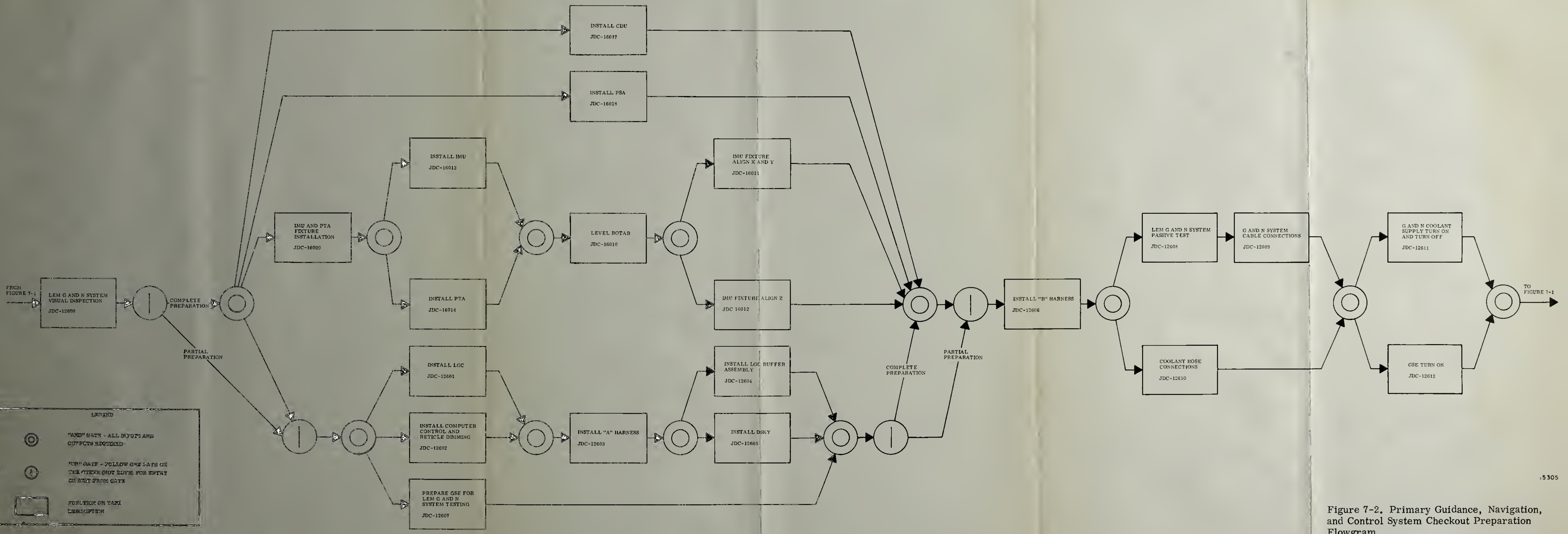

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Figure 7-2. Primary Guidance, Navigation, and Control System Checkout Preparation Flowgram

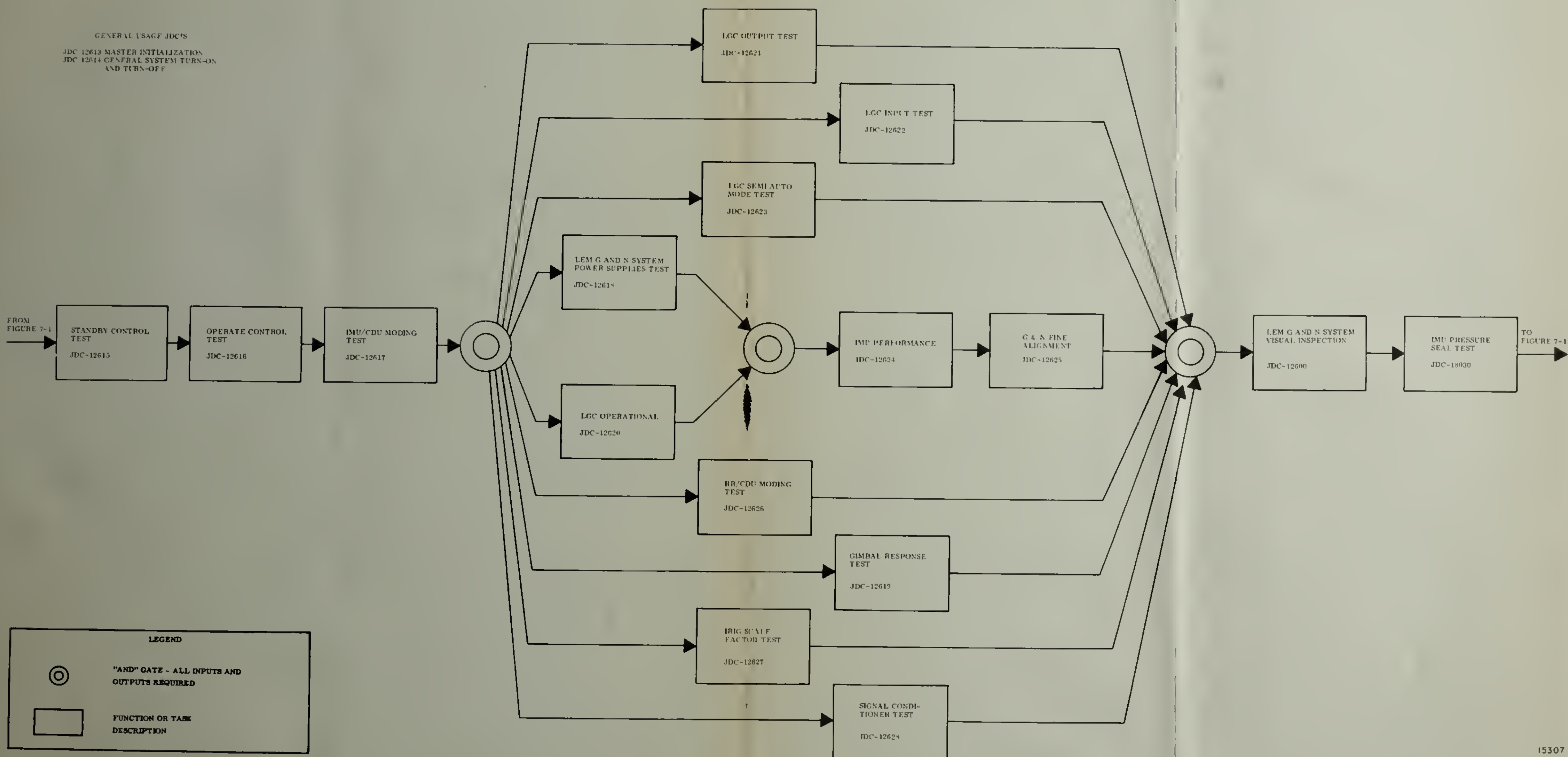

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Figure 7-3. Primary Guidance, Navigation, and Control System Checkout Flowgram

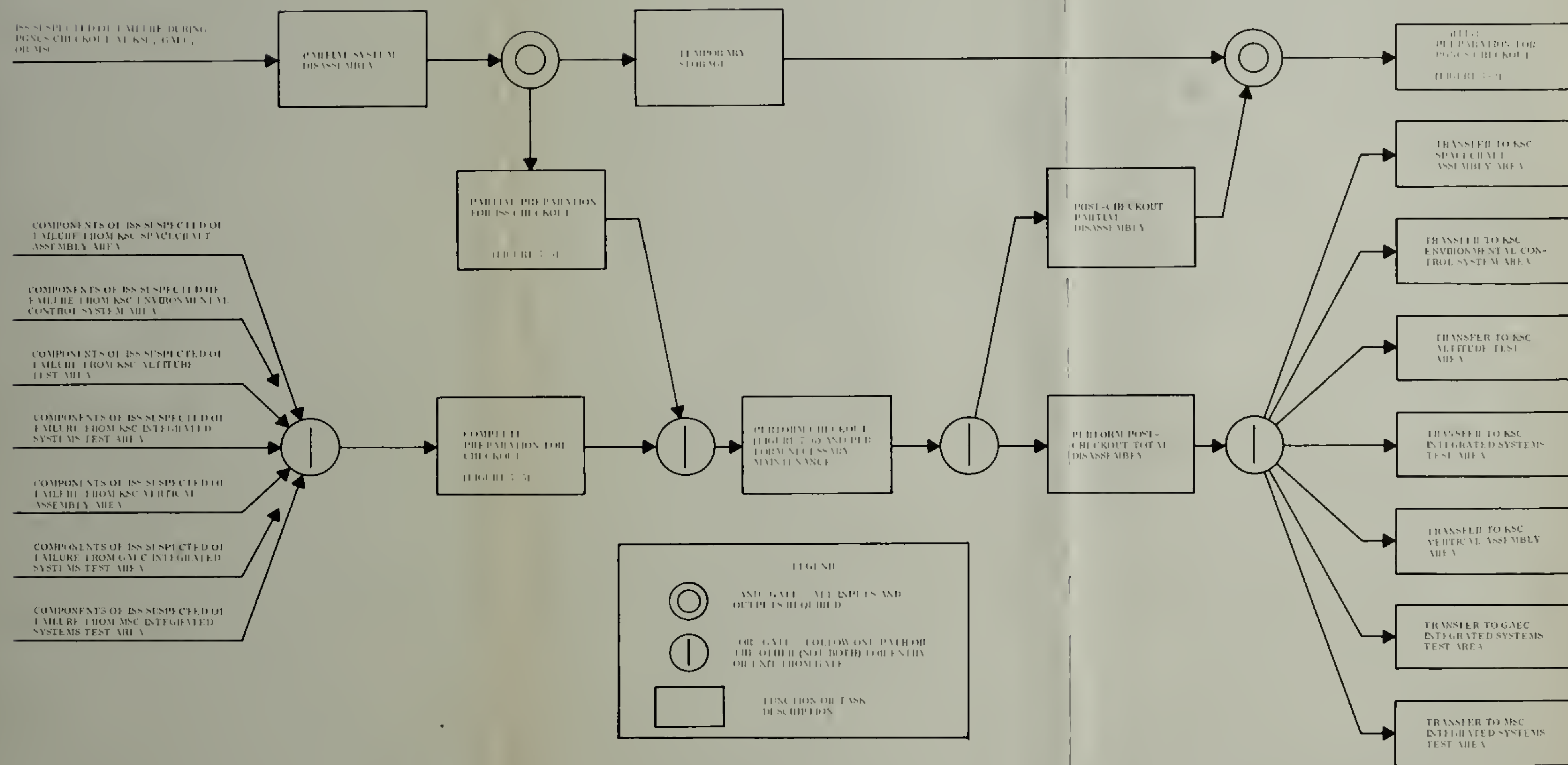

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Figure 7-4. Inertial Subsystem Master Checkout Flowgram

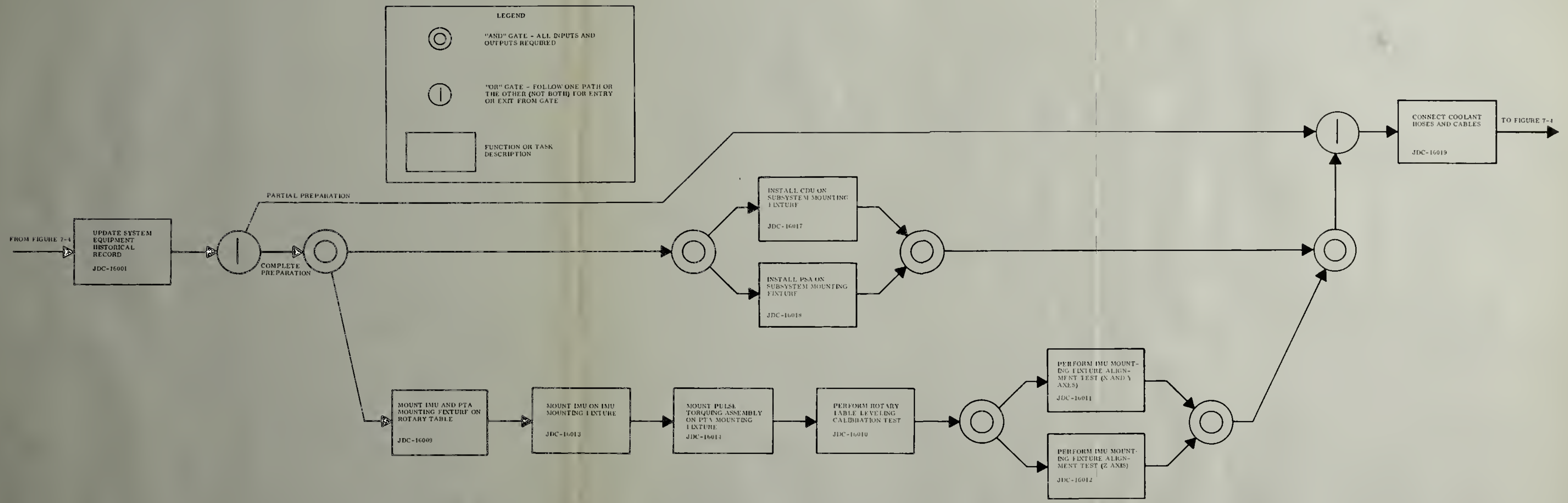

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Figure 7-5. Inertial Subsystem Checkout Preparation Flowgram

Figure 7-6. Inertial Subsystem Checkout Flowgram

Chapter 8

MAINTENANCE

8-1 SCOPE

This chapter describes maintenance for the LEM PGNCS at the Kennedy Space Center (KSC), Grumman Aircraft Engineering Corporation (GAEC) and North American Aviation (NAA). Job description cards (JDC's) are referenced as necessary to provide detailed instructions for checkout, removal, and replacement. Loop diagrams and schematics are referenced to aid malfunction isolation at system or subsystem level. In addition, chapter 8 contains a maintenance schedule and cleaning requirements for the PGNCS.

8-2 MAINTENANCE CONCEPT

Maintenance of the PGNCS at the KSC, GAEC, and NAA consists of the black box replacement method: replacement of only major components or assemblies. Equipment is received at field locations either as a complete PGNCS or as spare black boxes. In the event of failure during checkout of the PGNCS, the malfunction must be isolated to one of the following replaceable black boxes:

(1) CDU.

(2) IMU and matched PTA.

(3) PSA.

(4) LGC.

(5) DSKY.

(6) Flight ropes.

(7) Test ropes.

(8) Optical tracker.

(9) Luminous beacon.

(10) Nav base.

(11) Signal conditioner.

The maintenance flowgram (figure 8-1) presents the maintenance concept for the PGNCS. If a malfunction occurs, the following maintenance activities are performed:

(1) The PGNCS malfunction is isolated to a black box.

(2) The black box is retested sufficiently to verify that a malfunction exists.

(3) A spare black box is tested to insure that it is serviceable.

(4) The spare black box is installed in the PGNCS.

(5) The PGNCS is tested sufficiently to verify that repair is satisfactory.

(6) PGNCS checkout is resumed, starting with the JDC which originally failed.

8-3 MALFUNCTION ISOLATION

Malfunction isolation is performed by the engineer using GSE indications, PGNCS indications, loop diagrams, and schematics to isolate the malfunctioning black box.

The PGNCS and ISS loop diagrams and schematics required to perform malfunction isolation are listed in table 8-I. The CSS logic diagrams and schematics required to perform malfunction isolation are listed in table 8-II. The system and subsystem functional analysis in chapter 2, the component theory of operation in chapter 4, and the JDC test descriptions in chapter 7 are also useful in analyzing malfunctions.

If a malfunction cannot be isolated to a black box during PGNCS checkout, the checkout for the ISS, LORS, or CSS may be entered. Flowgrams in chapter 7 list the JDC's required to perform subsystem checkouts.

After malfunction isolation is completed, malfunction verification testing and pre-installation acceptance (PIA) testing are performed.

8-4 DOUBLE VERIFICATION

Each PGNCS malfunction will be doubly verified. The removed black box is tested to verify that a malfunction exists. The PGNCS is tested to verify that installation of a spare black box corrects the system malfunction.

8-4.1 MALFUNCTION VERIFICATION. Additional tests will be performed to verify that a malfunction exists in the black box. JDC's providing procedures for bench testing and partial subsystem testing of each black box will be listed in a table when information is available.

The malfunction verification JDC's are an aid to malfunction verification, and are used at the discretion of the engineer. However, specified pre-power assurance (PPA) tests of some black boxes will be required prior to further subsystem testing to prevent a black box malfunction from causing possible damage to the subsystem.

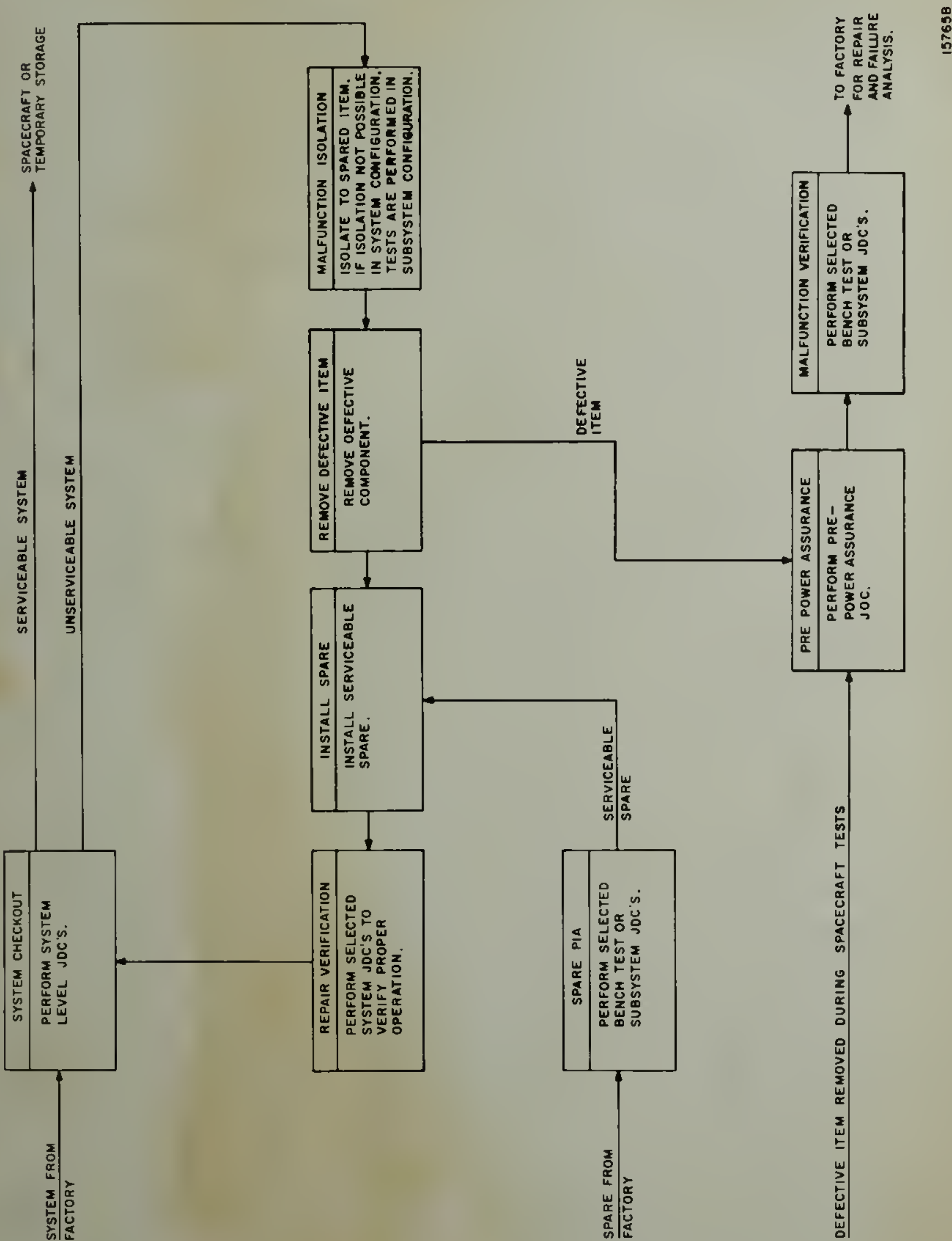


Figure 8-1. Maintenance Flowgram

Table 8-I. PGNCS and ISS Loop Diagrams and Schematics

Title	NASA Drawing
LEM +28 VDC Power Distribution	6015570
LEM 0 VDC Power Distribution	6015571
LEM +28 VDC 800 ~ Power Distribution	6015572
PTPS Output	6015573
Apollo Stab Loop - LEM	6015564
Apollo PIPA Loop - LEM	6015563
IMU-R/R CDU Block Diagram-Block II	2015566
LEM 5-Axis Moding Diagram	6015562
IMU Temperature Control System-Block II	2001452

Table 8-II. CSS Logic Diagrams and Schematics

Title	NASA Drawing
Tray A Subassembly	
Module A1	2005059
Module A2	2005060
Module A3	2005051
Module A4	2005062
Module A5	2005061
Module A6	2005063
Module A7	2005052
Module A8	2005055
Module A9	2005056
Module A10	2005057
Module A11	2005058
Module A12	2005053
Module A13	2005069
Module A14	2005064
Module A15	2005065
Module A16	2005066
Module A17	2005067
Module A18	2005068
Module A19	2005070
Module A20	2005054
Module A21	2005050
Module A22	2005071

(Sheet 1 of 2)

Table 8-II. CSS Logic Diagrams and Schematics

Title	NASA Drawing
Module A23	2005072
Module A24	2005073
Interface Module A25, A26	2005021
Interface Module A27-A29	2005020
Power Supply Module A30, A31	2005010
Tray B Subassembly	
Rope Memory Module B1-B6	2005012
Oscillator Module B7	2005003
Alarm Module B8	2005008
Erasable Driver Module B9, B10	2005004
Current Switch Module B11	2005005
Erasable Memory Module B12	2005006
Sense Amplifier Module B13, B14	2005002
Strand Select Module B15	2005009
Rope Driver Module B16, B17	2005000
DSKY	
DSKY Assembly	2005900
Indicator Driver Module D1-D6	2005902
Keyboard Module D8	2005903
Power Supply Module D7	2005904

(Sheet 2 of 2)

If a malfunction in the black box is verified, a spare black box, after passing a PIA test, is installed in the PGNCS. If no malfunction occurs during malfunction verification testing, a malfunction still exists in the PGNCS. The black box is reinstalled in the PGNCS and further malfunction isolation is required.

8-4.2 REPAIR VERIFICATION. After the malfunction has been verified, a PIA test completed, and a spare black box installed in the PGNCS, a partial system checkout is performed to verify that the PGNCS is repaired.

The JDC's required to perform repair verification after installation of a spare black box will be listed in a table when information is available. If no malfunction occurs during the specified tests, the PGNCS is repaired and system checkout may be resumed starting with the JDC which originally failed. If a malfunction occurs during repair verification testing, it is probable that a new malfunction exists or that more than one system malfunction existed originally.

8-5 PRE-INSTALLATION ACCEPTANCE TEST

A spare black box must pass a PIA test prior to installation in the PGNCS. A PIA test consists of performing a partial subsystem checkout or a bench test of the spare black box.

The standard test equipment and JDC's required to perform PIA for each black box will be referenced in a table when information is available. If no malfunction occurs during the specified procedures, the spare black box is acceptable for installation in the PGNCS. If a malfunction occurs during PIA testing, the black box is unsatisfactory and must be returned to the factory.

8-6 REMOVAL AND REPLACEMENT

The JDC's providing detailed instructions for removing and replacing black boxes in the PGNCS, ISS, LORS, and CSS will be referenced in a table when information is available.

8-7 MAINTENANCE SCHEDULE

The maintenance schedule will be provided when information is available.

8-8 OPTICAL CLEANING

Cleaning of the optics shall be performed only when necessary and with the approval of the responsible engineer. A JDC giving detailed cleaning instructions will be referenced when information is available.

Appendix A

LIST OF TECHNICAL TERMS AND ABBREVIATIONS

Term	Definition
a	Accelerometer
AAC	Automatic amplitude control
ACA	Attitude controller assembly
ACCEL	Accelerometer
ACE	Automatic checkout equipment
ACTY	Activity
A/D	Analog to digital
ADIA	Gyro drift due to acceleration along the input axis caused by an unbalance on the spin refcrence axis
ADSRA	Gyro drift due to acceleration along the spin reference axis caused by an unbalance on the input axis
AGC	Apollo guidance computer
AGC/OC	AGC CTS operation console
AGS	Abort guidance section
AIICR	Apollo integrated inventory and consumption report
A_{IG}	Inner gimbal angle
αB	Hypothetical rotation of the PIP case about its output axis equivalent to bias. Subscripts (X, Y, or Z) may be added to denote a specific PIP case rotation

Appendix A (cont)

Term	Definition
αX, αY, or αZ	Misalignment of PIP case about stable member axis. Subscripts (X, Y, or Z) may be added to denote a specific PIP case misalignment
A_{MG}	Middle gimbal angle
A_{OG}	Outer gimbal angle
ATCA	Attitude and translation control assembly
Att	Attitude
BD	Bias drift of IRIG. Subscripts (X, Y, or Z) may be added to denote a specific IRIG bias drift
CDU	Coupling data unit
CES	Control electronics section
CIS	Communications and Instrumentation System
CLR	Clear
CM	Command module
CMC	Command module computer
CSM	Command and service module
CSS	Computer subsystem
CTS	Computer test set
D/A	Digital to analog
DAC	Digital to analog converter
DECA	Descent engine control assembly
DSKY	Display and keyboard
ECS	Environmental control system
EPS	Electrical power system
ϵ_{IGA}	Inner gimbal axis error
ϵ_{IGR}	Inner gimbal resolver error

Appendix A (cont)

Term	Definition
ϵMGA	Middle gimbal axis error
ϵMGR	Middle gimbal resolver error
ϵOGR	Outer gimbal resolver error
ERR	Error
E(Xg)	X gyro error signal
E(Yg)	Y gyro error signal
E(Zg)	Z gyro error signal
FDAI	Flight director attitude indicator
g	Gyro
GAEC	Grumman Aircraft Engineering Corporation
γX, γY, or γZ	Misalignment of IRIG case about stable member corresponding axis. (First subscript denotes a specific gyro, second subscript is added to denote a specific stable member axis about which the gyro input axis is misaligned.)
G and N	Guidance and navigation
GSE	Ground support equipment
IA	Input axis
IG	Inner gimbal
IIP	Interrupt in process
IMU	Inertial measuring unit
IP	Interrogate pulse
IRIG	Inertial reference integrating gyro

Appendix A (cont)

Term	Definition
ISS	Inertial subsystem
JDC	Job description card
KSC	Kennedy Space Center
LEM	Lunar excursion module
LGC	LEM guidance computer
LORS	LEM optical rendezvous subsystem
LR	Landing radar
MCT	Memory cycle time
MG	Middle gimbal
MILA	Merritt Island Launch Area
MIT/IL	Massachusetts Institute of Technology Instrumentation Laboratory
MSC	Manned Spacecraft Center
N	Negative velocity pulse
NAA	North American Aviation
Nav	Navigation
nav base	Navigation base assembly
NBD	Normal bias drift
OA	Output axis
OG	Outer gimbal
OIA	Optics-inertial analyzer
OITS	Optics-inertial test set
OPR	Operator

Appendix A (cont)

Term	Definition
P	Positive velocity pulse
P_I	Incrementing pulse
PA	Pre-amplifier
PA	Pendulum axis
PAC	Program analyzer console
PCM	Pulse code modulated
PEA	PIPA electronics assembly
PGNCS	Primary guidance, navigation, and control system
ϕH_{MGA}	Corrected reading taken from the tilt axis optigon screen with rotary axis at θH_{OGA}, outer gimbal at precision zero, and middle gimbal axis in horizontal plane
ϕH_{RA}	Corrected reading taken from the tilt axis optigon screen with rotary axis in horizontal plane
PIA	Pre-installation acceptance
PIP	Pulsed integrating pendulum
PIPA	Pulsed integrating pendulum accelerometer
PLSS	Portable life support system
P&M	Programmer and monitor
PRA	Pendulum reference axis
PROG	Program
PSA	Power and servo assembly
PTA	Pulse torque assembly
PTC	Portable temperature controller

Appendix A (cont)

Term	Definition
PVR	Precision voltage reference
RCS	Reaction control system
REL	Release
RF	Radio frequency
RGA	Rate gyro assembly
RLC	Resistance inductance capacitance
RSET	Reset
S	Total gain from rotation about an IRIG input axis to voltage output of the preamplifier, (millivolts per milliradians). Subscripts (X, Y, or Z) may be added to denote a specific IRIG total gain voltage
SA	Servo amplifier
SCS	Stabilization and control system
SF(A)	Scale factor of PIP. Subscripts (X, Y, or Z) may be added to denote a specific PIP scale factor
SFTG	Scale factor of torque generator, (milliradians per pulse). Subscripts (X, Y, or Z) may be added to denote a specific IRIG torque generator scale factor
SG	Signal generator
SIDL	System identification data list
SM	Stable member
SP	Switch pulse
STBY	Standby
TCA	Translation controller assembly
TDCR	Technical data change request
TDCR-RB	Technical data change request review board

Appendix A (cont)

Term	Definition
TDRR	Technical data release or revision
TG	Torque generator
θH_{IGA}	Corrected reading taken from the rotary axis optigon screen with outer and middle gimbals at precision zero, and inner gimbal axis at local vertical
θH_{OGA}	Corrected reading taken from the rotary axis optigon screen with rotary axis horizontal and outer gimbal axis horizontal and east
$\theta + 1g$	True table rotary axis angle which places PIP input axis opposite local vertical vector. Subscripts (X, Y, or Z) may be added to denote a specific PIP input axis
$\theta - 1g$	True table rotary axis angle which places PIP input axis along local vertical vector. Subscripts (X, Y, or Z) may be added to denote a specific PIP input axis
TM	Torque motor
TPA	Test point adapter
T/W	Thrust-to-weight
V	Velocity

Appendix B

RELATED DOCUMENTATION

This appendix explains the function and relationship of the System Identification Data List (SIDL), the Apollo Integrated Inventory and Consumption Report (AIICR), the Aperture Card System, and the Technical Data Change Request Review Board (TDCR-RB) to the manual.

SIDL is an official release record for documents issued to implement NASA contracts. SIDL identifies drawings, specifications, manuals and job description cards (JDC's), and other documents released to support the LEM Primary Guidance, Navigation, and Control System (PGNCS).

Manuals and JDC's are based upon the latest information available as of the publication freeze date. Manuals and JDC's are distributed after formal CCB approval. SIDL shall be consulted to determine which is the currently effective information. AC Electronics, Field Service Publications Department, will periodically revise the manuals and JDC's to the latest technical information releases.

The AIICR is a listing of all approved spare parts for the PGNCS and its associated ground support equipment (GSE).

The aperture card system is a compilation of documents in the Apollo program. Each aperture card consists of a mounted 35 MM microfilm copy of a complete document, with the exception that for manuals, only the title page, signature page, record of revisions page, and list of effective pages are included to identify the revision letter, change pages, and TDRR number.

Aperture card sets are maintained at all field sites and are used with the PGNCS manual to refer to schematics, wiring diagrams, and other drawings which are not included in the manual.

The TDCR-RB is a group composed of AC Electronics Publications, Engineering, Field Operations, MIT/IL, and NASA personnel. The board meets as required to process and disposition Technical Data Change Requests (TDCR's).

Appendix C

LOGIC SYMBOLS

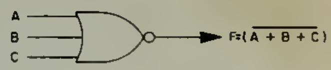
The LEM Guidance Computer contains NOR gates, extended NOR gates, and NOR gate flip-flops. For a better understanding of the logic used in the LGC, the logic symbols, terminology, and conventions used in logic descriptions in this chapter are discussed in detail in the following paragraphs.

The NOR gate (figure C-1) is a 3-input OR element with internal negation or inversion. This gate performs the logic function of $F = \overline{A + B + C}$, which is expressed as "neither A nor B nor C". From this the term NOR gate is derived.

The two more commonly used configurations of the NOR gate in the LGC are the AND and OR functions, also illustrated on figure C-1. The AND function ($\overline{A} \cdot \overline{B} \cdot \overline{C}$) is expressed as "not A and not B and not C". Another way of expressing this function is to state that an output is present when not A and B and C are coincident. An actual application of the AND function will demonstrate still another way of describing this configuration. The gate shown has as inputs the negations $\overline{\text{T09}}$ and $\overline{\text{XCH0}}$. The output function is described as: signal RP2 is generated at time 9 during an Exchange instruction. This means of describing the AND function will appear more frequently in text than the others. An OR function is simply the inverted result of a NOR function. The output function F is present if either A or B is present. If neither A nor B is present, the function F is not present.

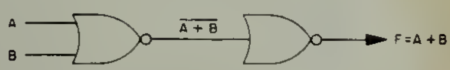
The extended NOR gate assumes the configuration shown on figure C-1. This is simply a method of increasing the number of inputs (fan-in) to produce a given function. On figure C-1 both gates are shown tangent to one another. They are drawn in this manner on many of the detailed logic drawings of this section since both gates follow in numerical sequence. However, both gates need not be, and on many drawings are not shown tangent to each other to produce the given function. The shaded portion of the lower gate indicates that it is an extension of the NOR gates shown above it through a common connection, which will be described in detail.

The NOR gate consists of three NPN transistors with resistive inputs, as shown in figure C-2. The collector of each transistor is connected to a common load resistor, the other end of which is connected to the +4 vdc supply. All three emitters are common

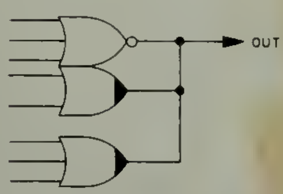


NOR GATE

AND FUNCTION



OR FUNCTION



EXTENDED NOR GATE

Figure C-1. NOR Gate Symbols

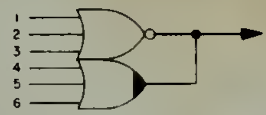
and are connected to ground. As a result of these connections, the logic levels for the LGC can be defined (+4 vdc represents a logic ONE; approximately ground level represents a logic ZERO). Since an NPN transistor requires a positive transition for turn-on, a logic ONE at any one input or at all three inputs results in a logic ZERO at the output. To correlate this to the NOR gate symbol of figure C-1, consider that inputs A, B, and C are each a logic ONE. The output is logic ZERO or the inverted form of the input.

When all three inputs to the NOR gate are each logic ZERO, the transistors are cutoff. The output assumes the collector supply voltage (+4 vdc) or logic ONE. This latter condition can be correlated to the AND function of the NOR gate in figure C-1. When the two inputs ($\overline{T09} \cdot \overline{XCH0}$) are each logic ZERO, the output (RP2) is a logic ONE. In the detailed discussions which follow, a logic ZERO level is often referred to as enabling an associated input gate leg. For example, the negation input $\overline{T09}$ enables the gate coincident with $\overline{XCH0}$ (both inputs logic ZERO). An input gate leg is considered to be a logic ZERO if there is no connection to that particular leg. Each NOR gate has a capacity of three inputs. If connections are made to only two inputs, the third is considered to be logic ZERO, or the leg is enabled.

The fan-in capacity is increased to produce a given function, as shown by the dotted connection on figure C-2. The extended gate has no connection through the common collector resistor to +4 vdc. Instead, the output from the extended gate is connected to the output line from the other gate. The collector resistor of this gate is now common to the transistors in both gates. This configuration does not change the logic ability of the gates. A logic ONE at any one or all of the six inputs results in a logic ZERO out. A logic ZERO at all six inputs results in a logic ONE out.

A NOR gate flip-flop consists of two NOR gates interconnected, as shown on figure C-3. The flip-flop is set by a logic ONE applied to the set input and is reset by a logic ONE applied to the reset input. The set pulse actually is applied to the reset side of the flip-flop; likewise the reset pulse is applied to the set side. This condition exists because of the characteristics of the NOR gate (a logic ONE at any input results in a logic ZERO out). The logic ZERO is applied to the input of the opposite side and holds that side off, which results in a logic ONE out. Thus, a set pulse applied to gate A of figure C-3 turns the gate on. The output of gate A (or the reset side) is a logic ZERO, which is applied to gate B and holds this gate off. The output of gate B (the set side) is a logic ONE.

The format used for each of the logic diagrams contained in the discussions in this manual is illustrated and explained on figure C-4.



EXTENDED NOR GATE SYMBOL

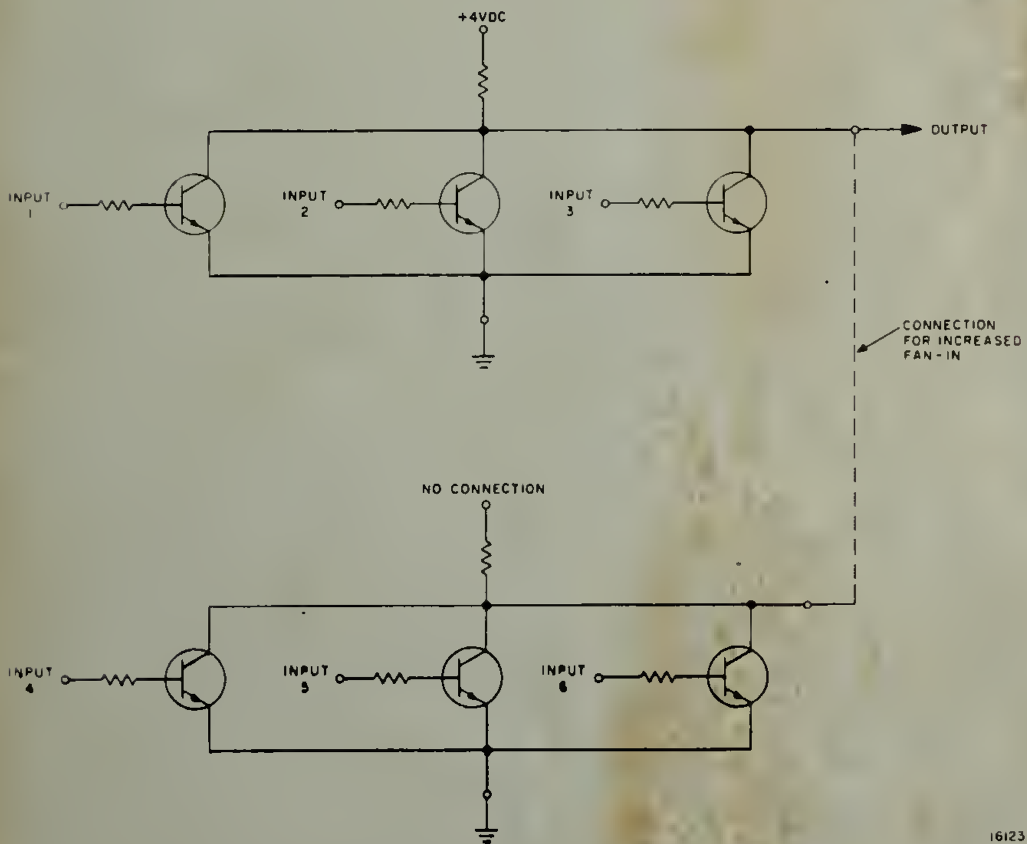


Figure C-2. NOR Gate Schematic

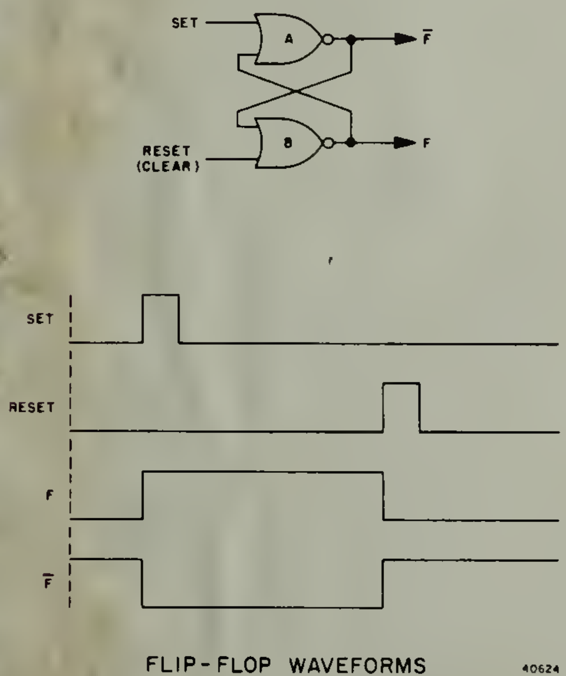
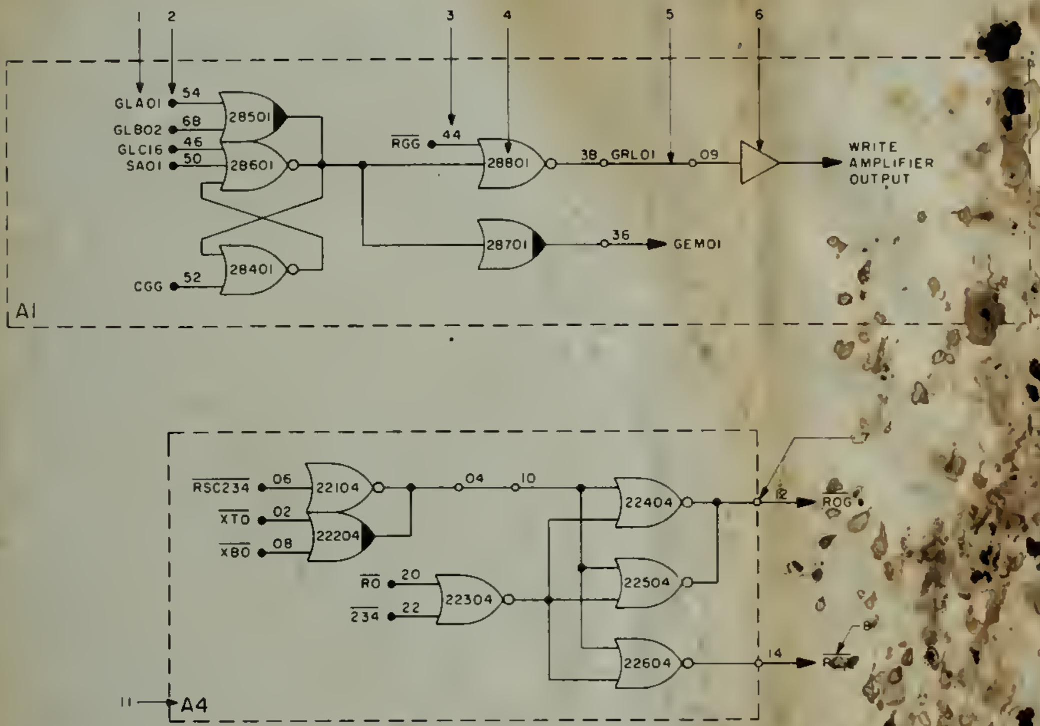


Figure C-3. NOR Gate Flip-Flop



KEY	
INDEX NUMBER	FUNCTION
1	INPUT SIGNAL
2	MODULE INPUT TERMINAL
3	MODULE INPUT TERMINAL NUMBER
4	CIRCUIT NUMBER
5	CONNECTION BETWEEN TERMINALS
6	WRITE AMPLIFIER
7	MODULE OUTPUT TERMINAL
8	OUTPUT SIGNAL
9	OUTPUT INTERFACE CIRCUIT
10	INPUT INTERFACE CIRCUIT
11	TRAY-MODULE DESIGNATION (LETTER DESIGNATES TRAY, NUMERAL DESIGNATES MODULE LOCATION)

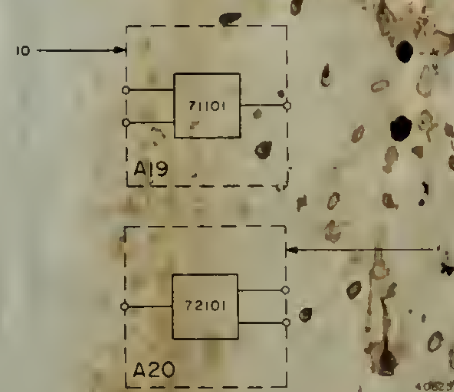


Figure C-4. Logic Diagram Symbols